GANDHI INSTITUTE OF TECHNOLOGY AND MANAGEMENT (GITAM)

(Deemed to be University)

VISAKHAPATNAM * HYDERABAD * BENGALURU

Accredited by NAAC with A^{++} Grade

GITAM School of Core Engineering

SYLLABUS

2 Year Postgraduate Programme
PEECE01: M.Tech. VLSI Design

w.e.f. 2024-25 Admitted Batch

(Updated on Nov 2024)

Academic Regulations

Applicable for the Postgraduate programmes in the School of Core Engineering

https://www.gitam.edu/academics/academic-regulations

Vision

To become a global leader in higher education.

Mission

To impart futuristic and comprehensive education of global standards with a high sense of discipline and social relevance in a serene and invigorating environment.

Quality Policy

To achieve global standards and excellence in teaching, research, and consultancy by creating an environment in which the faculty and students share a passion for creating, sharing and applying knowledge to continuously improve the quality of education.

GITAM School of Technology

Vision

To become a global leader in holistic engineering education and research

Mission

1. To impart a strong academic foundation and practical education through a flexible curriculum, state of the art infrastructure, and best learning resources

2. To actively pursue academic and collaborative research with industries and research institutions, both in India and abroad

3. To build a congenial and innovative eco system by enabling the latest technologies, thus helping the students, to solve the challenges of societal importance

4. To provide our students with the appropriate leadership, management, communication skills and professional ethics for career success and to continuously impact the global lives

Department of
Electrical, Electronics and Communication Engineering

VISION

To excel in higher education by imparting quality teaching and research and to meet the challenges in Electrical, Electronics and Communication Engineering

MISSION

1. To impart technical skills, value-based education to students, to enable them to face the demands of the industry
2. To create innovative and instructional learning methods to hone the skills for solving problems of society
3. To carry out research through constant interaction with R & D organizations and industry
4. To motivate the students to develop expertise in multidisciplinary technologies for a sustainable growth

PEECE01: M. Tech. VLSI Design

(w.e.f. 2022-23 Admitted Batch)

Program Educational Objectives

PEO1	To impart fundamental principles and design skills in integrated circuits, systems and signal processing
PEO2	To train students in using contemporary industry grade electronic design automation tools for VLSI design
PEO3	To expose students to latest developments in VLSI Design for pursuing research, formulating solutions to contemporary research problems of societal relevance
PEO4	To instil teamwork, leadership, and communication skills in the student with professional, ethical, and human values to be responsible citizen of the society

Programme Outcomes

Upon successful completion of MTech VLSI Design programme, students will be able to

PO1	design digital circuits and systems using programmable logic devices
PO2	analyze analog/digital circuits and systems using analytical and graphical device models
PO3	design analog/digital circuits balancing tradeoffs including area, power, speed and reliability
PO4	demonstrate the use of electronic design automation tools for designing integrated circuits using programmable logic, full custom and semi-custom design methodologies
PO5	apply research methods to formulate and solve research problems in integrated circuit design of contemporary relevance
PO6	describe the contemporary processes involved in the IC manufacturing process and analyze their implications in circuit design process
PO7	demonstrate soft skills, personality, ethics and learning enthusiasm in identifying and solving industry/research problems of contemporary relevance
PO8	survey and present state of the art circuit/system design procedures for VLSI Design and fabrication

M. Tech. VLSI Design

Department of Electrical, Electronic and Communication Engineering

Effective from academic year 2022-23 admitted batch

I Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EEC707	Digital System Design	CE	3	0	0	3
2	19EEC709	Digital IC Design	CE	3	0	0	3
3	19EEC711	Analog IC Design	CE	3	0	0	3
4	19EEC7XX	Program Elective-I	PE	3	0	0	3
5	19EEC7XX	Program Elective-II	PE	3	0	0	3
6	19EMC741	Research Methodology & IPR	MC	2	0	0	2
7	19EEC725	VLSI Circuit Design Laboratory	CE	0	0	4	2
8	19EEC727	FPGA Design Laboratory	CE	0	0	4	2
9	19EAC7XX	Audit Course I	AC	2	0	0	0
							21

II Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EEC706	VLSI Technology	CE	3	0	0	3
2	19EEC7XX	Program Elective –III	CE	3	0	0	3
3	19EEC7XX	Program Elective – IV	PE	3	0	0	3
4	19EEC7XX	Program Elective –V	PE	3	0	0	3
5	19EOE7XX	Open Elective	OE	3	0	0	3
6	19EEC792	Technical Seminar	CE	0	0	4	2
7	19EEC726	Advanced VLSI Design Laboratory	CE	0	0	4	2
8	19EEC728	IC Design Laboratory	CE	0	0	4	2
9	19EAC7XX	Audit Course II	AC	2	0	0	0
10	HSMCH102	Universal Human Values 2: Understanding Harmony*	HS	2	1	0	3
							24

* This course could also be offered during 3rd or 4th Semester

III Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EEC891	Project Work-I	Project	0	0	20	10
							10

IV Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EEC892	Project Work-II	Project	0	0	32	16
							16

M. Tech. VLSI Design
Number of Credits

Semester	I	II	III	IV	Total
Credits	21	24	10	16	**71**

AUDIT COURSES I & II

S.No	Course Code	Course Title	Category	L	T	P	C
1	19EAC741	English for Research Paper Writing	AC	2	0	0	0
2	19EAC742	Disaster Management	AC	2	0	0	0
3	19EAC743	Sanskrit for Technical Knowledge	AC	2	0	0	0
4	19EAC744	Value Education	AC	2	0	0	0
5	19EAC745	Constitution Of India	AC	2	0	0	0
6	19EAC746	Pedagogy Studies	AC	2	0	0	0
7	19EAC747	Stress Management by Yoga	AC	2	0	0	0
8	19EAC748	Personality Development through Life Enlightenment Skills	AC	2	0	0	0
9	19EAC750	Developing Soft Skills and Personality	AC	2	0	0	0

OPEN ELECTIVE

S.No	Course Code	Course Title	Category	L	T	P	C
1	19EOE742	Business Analytics	OE	3	0	0	3
2	19EOE746	Operations Research	OE	3	0	0	3

3	19EOE748	Cost Management of Engineering Projects	OE	3	0	0	3
4	19EOE752	Waste to Energy	OE	3	0	0	3
5	19EOE758	C Based VLSI Design	OE	3	0	0	3
6	19EOE756	Wind Energy	OE	3	0	0	3
7	19EOE762	Web Technologies	OE	3	0	0	3
8	19EOE764	Linux Programming and Scripting	OE	3	0	0	3

PROGRAMME ELECTIVES
(Choose any 5 courses under Programme Elective I – V)

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EEC753	Modeling and Design with HDLs	PE	3	0	0	3
2	19EEC755	Digital Signal Processing with FPGAs	PE	3	0	0	3
3	19EEC757	Semiconductor Device Modeling	PE	3	0	0	3
4	19EEC759	Semiconductor Devices	PE	3	0	0	3
5	19EEC761	VLSI DSP Architectures	PE	3	0	0	3
6	19EEC763	Active Filter Design	PE	3	0	0	3
7	19EEC760	RF IC Design	PE	3	0	0	3
8	19EEC762	Advanced Logic Synthesis	PE	3	0	0	3
9	19EEC764	Advanced Digital IC Design	PE	3	0	0	3
10	19EEC766	ASIC Design	PE	3	0	0	3
11	19EEC768	Broadband Communication Circuits	PE	3	0	0	3
12	19EEC770	Low Power VLSI Deign	PE	3	0	0	3
13	19EEC772	VLSI CAD	PE	3	0	0	3
14	19EEC774	Digital Systems Testing and Testability	PE	3	0	0	3
15	19EEC776	Data Converters	PE	3	0	0	3
16	19EEC778	Circuits for Analog System Design	PE	3	0	0	3
17	19EEC779	Computer Arithmetic	PE	3	0	0	3
18	19EEC780	Computer Architecture	PE	3	0	0	3
19	19EEC781	ARM System Development	PE	3	0	0	3
20	19EEC782	Advanced Computer Organization	PE	3	0	0	3
21	19EEC783	Operation and Modeling of MOS Transistor	PE	3	0	0	3
22	19EEC784	Digital Systems Engineering	PE	3	0	0	3
23	19EEC785	DSP Algoritshms and Implementations	PE	3	0	0	3
24	19EEC786	VLSI Physical Design Automation	PE	3	0	0	3
25	19EEC787	VLSI CAD	PE	3	0	0	3

19EEC707: DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

The emphasis of this course is on the design of digital systems and the use of a hardware description language, VHDL in the design process. Modeling the combinational and sequential logic circuits using basic features of VHDL is discussed and basics of the Programmable logic devices such as SPLDs, CPLDs and FPGAs are introduced in this course. This course also deals with the hardware implementation of the digital systems using programmable logic devices.

Course Objectives:

- To understand the basic concepts of designing combinational and sequential circuits and the possible hazards in the design.
- To model combinational and sequential circuits using VHDL.
- To design and model digital circuits using different modelling techniques and also design Finite State Machines.
- To study various programmable logic devices like SPLDs, CPLDs and FPGA. To study how to implement functions in FPGAs.

Unit I (8L)

Review of Logic Design Fundamentals: Combinational logic, Boolean algebra and algebraic Simplification, Karnaugh maps, designing with NAND and NOR gates, hazards in combinational circuits, flip-flops and latches, Mealy sequential circuit design, design of a Moore sequential circuit, equivalent states and reduction of state tables, sequential circuit timing, tristate logic and busses.

Learning Outcomes:

After completion of this unit, the student will be able to

- simplify the logic function using Boolean algebra and Karnaugh maps (L2).
- design combinational and sequential logic circuits using NAND/NOR gates (L4).
- design Mealy and Moore finite state machines for the given specifications (L4).
- analyze the timing characteristics of a given sequential logic circuit (L3).

Unit II (10L)

Introduction to VHDL: Computer-aided design, hardware description languages, VHDL description of combinational circuits, VHDL modules, sequential statements and VHDL processes, modeling flip-flops using VHDL processes, processes using wait statements, two types of VHDL delays: Transport and inertial delays, compilation, simulation, and synthesis of VHDL code, VHDL data types and operators, simple synthesis examples, VHDL models for multiplexers, VHDL libraries, modeling registers and counters using VHDL processes, behavioral and structural VHDL, variables, signals, and constants, assert and report statements.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the basics of VHDL (L1).
- describe a digital circuit at different levels such as behavioral, dataflow and structural (L2).
- describe the behavior of combinational and sequential logic circuits using VHDL processes (L2).

- understand different types of delays in VHDL (L1).

Unit III **(8L)**

Introduction to Programmable Logic Devices: Brief overview of programmable logic devices, simple programmable logic devices (SPLDs), complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), Design Examples: BCD to 7-segment display decoder, a BCD adder, 32-bit adders, traffic light controller, state graphs for control circuits, synchronization and debouncing, a shift-and-add multiplier, array multiplier.

Learning Outcomes:

After completion of this unit, the student will be able to

- explain the capabilities of different programmable logic devices (L2).
- implement the combinational and sequential logic circuits using PLDs (L4).
- distinguish between different programmable logic devices (L2).
- design and model different types of control circuits using VHDL (L5).

Unit IV **(6L)**

SM Charts and Microprogramming: State machine charts, derivation of SM charts, realization of SM charts, implementation of the dice game, microprogramming

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the components of state machine charts (L1).
- develop the state machine charts for a given digital data processing (L3).
- understand the realization of the SM charts (L3).
- implement the digital circuits using microprogramming (L5).

Unit V **(8L)**

Designing with Field Programmable Gate Arrays: Implementing functions in FPGAs, implementing functions using Shannon's decomposition, carry chains in FPGAs, cascade chains in FPGAs, examples of logic blocks in commercial FPGAs, dedicated memory in FPGAs, dedicated multipliers in FPGAs, cost of programmability, FPGAs and One-Hot state assignment.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the shannon's expansion theorem to decompose functions (L2).
- implement Boolean functions in FPGA devices using cascade chains and carry chains (L4).
- implement Boolean functions in FPGA devices using one-hot state assignment (L4).
- estimate the performance factors of the digital system such as delay, area and power (L3).

Text Book

1. Charles Roth, Digital Systems Design using VHDL, 2/e, Cengage Learning, 2012.

References

1. John F. Wakerly, Digital Design Principles and Practices, 4/e, Pearson Education, 2013.

2. Michael Ciletti, Advanced Digital Design using Verilog HDL, 2/e, Prentice Hall Publications, 2012.
3. Stephen Brown, ZvonkoVranesic, Fundamentals of Digital Logic with Verilog Design, 2/e, Tata McGraw Hill Publishers, 2014.

Course Outcomes:

After successful completion of the course, the student will be able to

- Design a combinational and sequential logic circuits with the help of K-maps using NAND/NOR/Universal gates (L4).
- Design mealy and moore state machines for the given specifications (L4). Analyze the timing characteristics of a given sequential logic circuit (L3).
- Understand the basics of VHDL (L1).
- Develop VHDL models of combinational and sequential logic circuits (L2).
- Distinguish between different programmable logic devices (L3).
- Develop the state machine charts for a given digital data processing (L3).
- Implement Boolean functions in FPGA devices using cascade chains, one-hot assignment etc (L5).

19EEC709: DIGITAL IC DESIGN

L T P C
3 0 0 3

This course is focused on applications of digital CMOS circuits and to understand the fabrication process of CMOS technology. Design of combinational and sequential circuits and implementation of the circuits with the help of FPGA, CPLD and some other form of devices is discussed.

Course Objectives

- To explain the operation of different MOS transistors and their characteristics like I-V and C-V characteristics.
- To discuss basic CMOS logic gates, implementation of multiplexers using tristate gates.
- To analyze different delays and power dissipation in number of stages.
- To understand the design of combinational circuits using ratioed, cascade and dynamic logic.
- To design different types of sequential circuits.

Unit I **(8L)**

MOS Transistor Theory: A Brief History, MOS Transistors, Long-Channel I-V Characteristics, C-V Characteristics, Non ideal I-V, Device Models.

Learning Outcomes:

After completion of this unit the student will be able to

- describe enhancement NMOS operation with neat diagrams (L1).
- discuss the brief history of CMOS VLSI design (L2).
- explain about CMOS operation and fabrication steps with relevant figures (L5).
- analyze the relation between Ids verses Vds for long channel ideal I-V characteristics of NMOS transistor (L4).

Unit II **(8L)**

Logic gates: CMOS Logic Gates (The Inverter, NAND and NOR Gate, Compound Gates), Pass Transistors and Transmission Gates Tristate, Tristate, Multiplexers, Sequential Circuits.

Learning Outcomes:

After completion of this unit the student will be able to

- design X=A`B+AB` using CMOS logic gate (L5).
- explain about pass transistor and transmission gate (L2).
- discuss 4X1 multiplexer using tri-state logic (L2).
- construct D-Flip Flop using CMOS logic (L3).

Unit III **(8L)**

Delay & Power calculations: RC Delay Model, Linear Delay Model, Delay in Multistage Logic Networks, Choosing the Best Number of Stages, Dynamic Power, Static Power. **Learning Outcomes:**

After completion of this unit the student will be able to

- state the different delays like RC delay and Linear delay (L1).

- understand the calculation of delays in multi stage logic circuits (L2).
- determine static and dynamic power in different stages of MOS circuits (L3).

Unit IV **(8L)**

Design of combinational circuits: Static CMOS, Rationed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass-Transistor Circuits.

Learning Outcomes

After completion of this unit the student will be able to

- describe about different static CMOS designs (L1).
- explain different pass-transistor circuits (L2).
- discuss about (i) Pseudo NMOS (ii) Cascode voltage switch (L2).
- illustrate domino logic using dynamic circuits (L3).

Unit V **(8L)**

Design of sequential circuits: Conventional CMOS Latches &Flip-Flops, Pulsed Latches, Resettable Latches and Flip-Flops, Enabled Latches and Flip-Flops, Incorporating Logic into Latches, Differential Flip-Flops, Dual EdgeTriggered Flip-Flops True Single-Phase-Clock (TSPC) Latches and Flip-Flops.

Learning Outcomes:

After completion of this unit the student will be able to

- identify differentiate between conventional CMOS latches and flip-flops (L1).
- explain about enabled latches and flip-flops (L2).
- analyze about true single phase clock latches and flip-flops (L4).
- design various approaches to implement an edge triggered flip-flops (L5).

Text book:

1. Weste, N. H. E., Harris, D. M (2005). CMOS VLSI design: a circuits and systems perspective. Boston, Pearson/Addison-Wesley.

References

1. S. M. Kang, Y. Leblebici, CMOS Digital Integrated Circuits, 3/e, McGraw Hill, 2012.
2. Jackson, Hodges, Analysis and Design of Digital Integrated circuits, 3/e, McGraw Hill, 2012. 3. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2011

Course Outcomes:

After successful completion of the course, the student will be able to

- understand the fundamental areas of applications for the Integrated Circuits (L1).
- identify the basic design structures using CMOS logic (L4).
- design the different delays like RC, Linear etc and to know how to calculate static and dynamic power (L5).
- analyze to draw different ratioed logic circuits and cascade circuits (L4).

19EEC711: Analog IC Design

L T P C
3 0 0 3

This course introduces the student, to the fundamentals of MOS device physics and building blocks of analog integrated circuit design. The first unit cover basics of MOS device physics. Units 2 and 3 covers different amplifiers used in analog IC design. Unit 4 covers the frequency response of amplifiers and feedback mechanisms used in different amplifiers. The last unit covers operational amplifier and its frequency compensation.

Course Objectives:

- To understand the construction, operation and mathematical models of MOSFETs.
- To analyze and design single stage and multistage amplifiers at low frequencies.
- To study and analyze different current mirrors used to bias IC amplifiers.
- To understand the frequency response of amplifier designed in integrated circuits.
- To understand the principles of operation of different feedback topologies.
- To understand different specifications and topologies related to operational amplifiers.

Unit I **(8L)**

Basic MOS Device Physics: General considerations, MOSFET as a switch, MOSFET structure, MOS symbols, MOS I/V characteristics, threshold voltage, derivation of I/V characteristics, second-order effects, MOS device models, MOS device layout, MOS device capacitances, MOS small-signal model, MOS SPICE models, NMOS versus PMOS devices, long-channel versus short-channel devices.

Learning Outcomes:

After completion of this unit the student will be able to

- understand and identify different operating regions of MOSFET (L1).
- understand the MOS device Models used in small-signals (L2).
- understand the MOS device Capacitances (L2).

Unit II **(8L)**

Single-Stage Amplifiers: Basic concepts, common-source stage, common-source stage with resistive load, CS stage with diode-connected load, CS stage with current-source load, CS stage with triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, folded cascode, choice of device models.

Learning Outcomes:

After completion of this unit the student will be able to

- identify different amplifiers using MOSFET (L2).
- analyze and design different amplifiers using MOSFET (L2).

Unit III **(8L)**

Differential Amplifiers: Single-ended and differential operation, basic differential pair, qualitative analysis, quantitative analysis, common-mode response, differential pair with MOS loads, gilbert cell. **Passive and Active Current Mirrors:** Basic current mirrors, cascode current

mirrors, active current mirrors, large-signal analysis, small-signal analysis, common-mode properties.

Learning Outcomes:

After completion of this unit the student will be able to

- analyze and design differential amplifiers using MOSFET (L2).
- analyze and design active and passive current mirrors using MOSFETs (L3).

Unit IV **(8L)**

Frequency Response of Amplifiers: General considerations, Miller effect, association of poles with nodes, common-source stage, source followers, common-gate stage, cascode stage, differential pair. **Feedback:** General considerations, properties of feedback circuits, types of amplifiers, feedback topologies, voltage-voltage feedback, current-voltage feedback, voltage-current feedback, current-current feedback, effect of loading, two-port network models, loading in voltage-voltage feedback.

Learning Outcomes:

After completion of this unit the student will be able to

- understand the frequency response of single stage and differential amplifiers using MOSFETs (L4).
- understand different feedback topologies used in amplifiers (L2).
- understand different two-port networks used to analyze feedbacks (L2).

Unit V **(8L)**

Operational Amplifiers: General considerations, performance parameters, one-stage op amps, two-stage op amps, gain boosting, comparison, common-mode feedback, input range limitations, slew rate, power supply rejection. **Stability and Frequency Compensation:** General considerations, multipole systems, phase margin, frequency compensation, compensation of two-stage op amps.

Learning Outcomes

After completion of this unit the student will be able to

- understand performance parameters related to operational amplifiers (L2).
- understand the working of different operational amplifier topologies (L2).
- analyze and design different operational amplifiers for the given specifications (L4).
- understand the stability and frequency compensation in operational amplifiers (L3).

Text Books

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2011.

References

1. P. R. Gray & R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5/e, John Wiley, 2012.
2. Ken Martin, Analog Integrated Circuit Design, 2/e, Wiley Publications, 2012.
3. Sedra and Smith, Microelectronic Circuits, 6/e, Oxford Publications, 2014.

Course Outcomes:

After successful completion of the course, the student will be able to

- acquire knowledge of device physics related to MOSFET (L1).
- acquire knowledge of amplifier design with the use of proper biasing techniques (L2).
- identify appropriate circuit topology for given gain, input impedance, output impedance and bandwidth requirements (L2).
- design single and multi-stage amplifiers for desired gain, bandwidth and terminal impedance specifications (L4).
- design feedback circuits to meet the given gain error, bandwidth, input and output impedance requirements (L4).
- acquire the knowledge of different op-amp topologies and to design op-amps for the given specifications (L3).

19EEC753: MODELING AND DESIGN WITH HDLs

L T P C
3 0 0 3

This course introduces the student, to Design digital logic using Verilog HDL. The first three units cover various modeling styles in Verilog. The fourth unit describes various design examples in Verilog. The last unit describes use of Testbench and Verification in VLSI using System Verilog.

Course Objectives:

- To familiarize the Digital Design using Verilog HDL.
- To explain various syntax and semantics of Verilog HDL.
- To describe various modeling styles in Verilog HDL.
- To impart the knowledge of designing Digital logic using various examples in Verilog HDL.
  - To introduce the Testbench and use of verification using System Verilog.

Unit I **8L**

Basic Concepts: Lexical conventions, data types, system tasks and compiler directives. **Modules and Ports:** Modules, ports, hierarchical names. **Gate-Level Modeling:** Gate types, gate delays.

Learning Outcomes:

After completion of this unit the student will be able to

- identify various lexical convention and data types (L2).
- understand various System tasks and Compilers (L2).
- state and define Modules and ports (L2).
- determine gate-level modeling with gate types and delays (L3).
- apply digital logic design using gate-level modeling (L4).

Unit II **8L**

Dataflow Modeling: Continuous assignments, delays, expressions, operators, and operands, operator types, examples.

Learning Outcomes:

After completion of this unit the student will be able to

- state continuous assignment, operators (L2).
- identify various operators (L2).
- predict the use of delay, expression and operators (L2).
- determine the operator precedence (L2).
- apply dataflow modeling style for digital design (L4).

Unit III **8L**

Behavioral Modeling: Structured procedures, procedural assignments, timing controls, conditional statements, multiway branching, loops, sequential and parallel blocks, generate blocks, examples.

Learning Outcomes:

After completion of this unit the student will be able to

- state procedural assignment, sequential & parallel blocks and generate blocks (L2).
- identify timing control and conditional statements (L2).
- predict the use of multiway branching and loops (L2).
- determine the use of generate block (L2).
- apply behavioral modeling style for digital design (L4).

Unit IV **8L**

Design examples: Difference between tasks and functions **Timing and Delays**: Types of delay models, path delay modeling, timing checks, delay back annotation, BCD to 7-Segment Display Decoder, BCD Adder,32-Bit Adders, Traffic Light Controller, Shift-and-Add Multiplier, Array Multiplier.

Learning Outcomes:

After completion of this unit the student will be able to

- state the difference between tasks and functions (L2).
- identify timings and delays using example (L2).
- predict the use of multiway branching and loops (L2).
- determine the use of generate control and data path with example (L3).
- apply different modeling style to design adders and multipliers (L4).

Unit V **8L**

Writing Test benches using System Verilog:

What is Verification, what is a Test bench, The Importance of Verification, Convergence Model, What Is Being Verified, Functional Verification Approaches, Testing Versus Verification, Design and Verification Reuse, The
Cost of Verification

Learning Outcomes:

After completion of this unit the student will be able to

- state verification and Testbench (L5).
- identify the importance of verification and convergence model (L5).
- predict cost of verification (L5).
- determine functional verification approaches (L5). □ apply design and verification reuse (L5).

Text Book(s)

1. Samir Palnitkar, Verilog HDL, 2/e, Pearson Education, 2013.
2. Charles Roth, Digital Systems Design using Verilog, Cengage Learning, 2014

References

1. Janick Bergeron, “Writing Test benches using System Verilog”, Springer.
2. J. Bhasker, System Verilog HDL Primer, B.S. Publications, 2012.
3. J. Bhasker, Verilog Synthesis Primer, B. S. Publications, 2011.
1. M. Ciletti, Advanced Digital Design with Verilog HDL, 2/e. Pearson Education, 2012.

Course Outcomes:

After successful completion of the course, the student will be able to describe the basic concepts in Verilog HDL (L2).

- list and describe various modeling style in Verilog HDL (L3).
- compare and identify Gate, Dataflow and Behavioral modeling using digital design examples (L4).
- analyze and design combinational and sequential circuits in Verilog (L1).
- explain the principles and operation test bench and verification using System Verilog (L5).

19EEC755: DIGITAL SIGNAL PROCESSING WITH FPGAs

L T P C
3 0 0 3

This course introduces the student, FPGA Architectures and implementation of digital signal processing algorithms on FPGAs. The first two units introduce fundamentals of DSP, FPGA and programmable signal processors, data representation, fixed-point and floating-point representations, Data path subsystems, binary adders and multipliers, and Digital Filter designs.

Course Objectives:

- To introduce Data-path subsystem design and illustrate their applications in implementing DSP algorithms. To familiarize with FIR and IIR filter designs and implementations.
- To explain about the fundamentals of Multirate Signal Processing algorithms and techniques, and illustrate their applications for filter design.
- To illustrate the importance of FFT for Fourier transform computation, and introduce FFT algorithms for computing DCT.
- To introduce Adaptive systems and their applications for signal detection and estimation, and illustrate algorithms for estimation.
- To introduce error control coding and coding theory, and various types of codes, like block codes and convolutional codes.

Unit I **8L**

Introduction: Overview of digital signal processing, FPGA technology, DSP technology requirements, FPGA and programmable signal processors. **Computer Arithmetic:** Number representation, fixed-point numbers, unconventional fixed-point numbers, floating-point numbers, and binary adders, pipelined adders, modulo adders, binary multipliers, multiplier blocks, fixed-point arithmetic implementation, and floating-point arithmetic implementation.

Learning Outcomes:
After completion of this unit, the student will be able to

- understand FPGA Technology and DSP processors (L1).
- analyze Fixed-point and Floating-point number representations, and their formats (L1).
- analyze and design Data-path subsystems, like Adders and Multipliers (L2).
- design and analyze, Fixed-point and Floating-point arithmetic implementations of Data-path subsystems (L3).

Unit II **8L**

FIR Filters: Digital filters, FIR theory, designing FIR filters, constant coefficient FIR design. **IIR Filters:** IIR coefficient computation, IIR filter implementation, Fast IIR filter.

Learning Outcomes:
After completion of this unit, the student will be able to

- design FIR and IIR filters (L1).
- characterize the performance of FPGA implementations of FIR and IIR filters (L2).
- implement various digital filter architectures in MATLAB or any ECAD tool (L3).

- explain IIR filter architectures and discriminate their performance characteristics from FIR filters (L3).

Unit III **8L**

Multirate Signal Processing: Decimation and interpolation, polyphase decomposition, Hogenaur CIC filters. **Fourier Transforms:** DFT algorithms, FFT algorithms, computing DCT using FFT.

Learning Outcomes:

After completion of this unit, the student will be able to

- apply concepts of Multirate signal processing for practical DSP systems (L1).
- implement FFT algorithms on FPGA and their characterization (L2).
- realize DCT and characterize their performance (L3).
- explain Radix-n FFT algorithms (L4).
- explain the implementation of DCT using FFT (L5).

Unit IV **8L**

Adaptive Systems: Application of adaptive systems, optimum estimation techniques, LMS algorithm, transform domain LMS algorithms, implementation of the LMS algorithm.

Learning Outcomes:

After completion of this unit, the student will be able to

- explain Adaptive systems and their implementations (L1 & L2).
- realize LMS algorithm and its variants(L3).
- implement an application based on LMS algorithm, with the prime objective of optimizing the performance (L4).

Unit V **8L**

Communication Systems: Error control, basic concepts from coding theory, block codes, convolutional codes, modulation and demodulation.

Learning Outcomes:

After completion of this unit, the student will be able to

- explain "Error control techniques" (L1).
- understand basic concepts from coding theory (L2).
- explain about block and convolutional codes (L3).
- understand Modulation and Demodulation techniques (L4).
- realize coding theory and concepts for any practical case (L5).

Text Book

1. Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, 4/e, Springer Publications, 2014

References

1. Roger Woods, John McAllister, Dr. Ying Yi, FPGA-based Implementation of Signal Processing Systems, Wiley Publications, 2011.
2. Shoab Ahmed Khan, Digital Design of Signal Processing Systems, Wiley Publications, 2011.
3. KeshabParhi, VLSI Digital Signal Processing, Wiley Student Edition, 2010.

Course Outcomes:

After successful completion of the course, the student will be able to

- implement digital filter designs on FPGA (L1).
- explore adaptive systems for optimizing the performance of a DSP system (L3).
- identify various Error control techniques and coding theory (L2).
- developing FPGA prototypes for DSP algorithms, for speech and image processing applications (L4).
- design and develop innovative techniques for realizing DSP algorithms (L5).

19EEC757: SEMICONDUCTOR DEVICE MODELING

L T P C
3 0 0 3

This course introduces the student, foundations of Semiconductor device physics, and operating principles of Semiconductor devices, PN junction diode, MIS Junction, BJTs and FETs and device modeling approaches.

Course Objectives

- To introduce the concepts of semiconductor physics and explain them briefly.
- To analyze and design Semiconductor devices, with a focus on more realistic phenomenon.
- To understand static and dynamic behavior of Semiconductor devices, and analyze their importance for device design.
- To introduce non-ideal conditions and their influence on C-V characteristics in MIS capacitor.
- To introduce the physical operation principle of BJT and their static characteristics.
- To introduce the physical operation principle of JFET, MESFET and MISFET, and their static characteristics.
- To introduce small-signal modeling and derive small signal equivalent circuit of various Semiconductor devices.

Unit – I **8L**

Concentration and motion of carriers in Semiconductor bulk - equilibrium concentration in intrinsic and extrinsic semiconductors, excess carriers, drift and diffusion transport, continuity equation. Concentration and motion of carriers at the interface - surface recombination, surface mobility etc.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand carrier statistics in Semiconductors (L1).
- explain intrinsic and extrinsic Semiconductors, and analyze the carrier concentrations and understanding their importance on their working(L1).
- understand the carrier transport in Semiconductors, such as drift and diffusion transport and their implications on current through Semiconductors (L2).
- interpret the continuity equation for various operating conditions in Semiconductors (L3).
- to explain about carrier concentrations at the interface and surface mobility, understanding their implication on the device behavior, like MOSFETs (L5).

Unit – II **10L**

Device modeling - basic equations for device analysis, approximation to these equations for deriving analytical expressions.PN homojunction - ideal static I-V characteristics and deviations including breakdown, ac small signal equivalent circuit, switching characteristics.

Learning Outcomes

After completion of this unit, the student will be able to

- solve basic equations for understanding and analyzing Semiconductor devices (L1).
- understand the importance of approximations for simplifying the basic equations for analyzing Semiconductor devices (L2).
- understand the cases when and where the approximations can be used for analyzing Semiconductor devices (L3).
- identify Semiconductor device modeling foundation for characterizing and designing Analog/Digital circuits (L4).
- understand the physical operation of PN junctions (L1).
- explain and interpret static I-V characteristics of PN junctions (L2).
- analyze PN junctions under non ideal conditions (L3).
- understand the small signal equivalent circuit of PN Junction diode (L3).
- explain switching characteristics of PN Junction and explore the design space of PN junctions (L4).

Unit – III **8L**

MIS Junction/capacitor - ideal C-V characteristics and deviations due to interface states/charges and work function differences, threshold voltage.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the electrostatics of MIS Junction/Capacitor under ideal conditions (L1).
- understand the electrostatics of MIS Junction/Capacitor under non ideal conditions, due to interface states and work function differences (L2).
- analyze the threshold voltage of MIS Junction under non ideal conditions (L3 & L4).

Unit – IV **8L**

BJT - transistor action, static characteristics, ac small signal equivalent circuit, switching characteristics.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the physical operation and electrostatics of BJT under ideal conditions (L1).
- analyze the BJT operation for various operating modes, Forward active, Saturation and Cutoff modes (L2). □ derive the small signal equivalent circuit and identify its importance for circuit design and analysis (L3).
- explain switching characteristics of BJTs and explore the design space by employing BJTs as switching elements (L4).

Unit – V **8L**

FETs - field effect, types of transistors (JFET, MESFET, and MISFET), static characteristics of MISFET, small signal equivalent circuit, difference between BJT and FETS.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the physical operation of FETs and identify the important differences between BJTs and FETs (L1).
- analyze the static behavior of JFET and MESFET, and deriving the small signal parameters (L2).
- derive the small signal model from the foundations of small signal analysis, for JFET and MESFET (L3).
- interpret the applicability of small signal model of JFET or MESFET, for various operating conditions (L4).

Textbook(s):

1. M. Lundstrom, "Fundamentals of Carrier Transport", Cambridge University Press, 2000.
2. C. Snowden, "Introduction to Semiconductor Device Modeling", World Scientific, 1986.

References

1. Y. Tsividis and C. McAndrew, "MOSFET modeling for Circuit Simulation", Oxford University Press, 2011.
2. BSIM Manuals available on BSIM homepage on the internet.
3. T. A. Fjeldly, T. Ytterdal and M. Shur, "Introduction to Device Modeling and Circuit Simulation", John Wiley, 1998.
4. Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 1998.
5. Shreepad karmalkar, NPTEL Video Course on "Semiconductor Device Modeling", http://nptel.ac.in/courses/117106033/

Course Outcomes:

After successful completion of the course, the student will be able to

- analyze the basic device equations and understanding their importance for analyzing the device behavior (L1).
- analyze the DC and small signal behavior of Semiconductor devices and utilizing their small signal models for circuit analysis and design (L3).
- explain the switching characteristics of Semiconductor devices (L2).
- design Semiconductor devices for the given performance specifications (L3).
- apply the concepts of small signal modeling for Semiconductor devices (L4).
- interpret data sheets of various semiconductor devices and bring out the required one for the given application (L5).

19EEC759: SEMICONDUCTOR DEVICES

L T P C
3 0 0 3

This course introduces the students to the physics of semiconductors and the inner working of semiconductor devices. The first unit covers band structures of different materials, carrier transport mechanisms and their effects. The other four units cover different semiconductor devices and technologies.

Course Objectives:

- To determine the band structure of semiconductors when supplied with basic materials properties and applying their knowledge of quantum mechanics.
- To calculate carrier distributions in thermal equilibrium and non-thermal equilibrium conditions for intrinsic and doped semiconductors.
- To apply basic semiconductor drift-diffusion equations to determine current flow in semiconductor devices.
- To differentiate between the fundamental difference of p/n junctions and field effect transistors.
- To determine alignment of metal-semiconductor band diagrams and identify whether junction is Ohmic or Schottky.
- To Design a bipolar transistor, metal-oxide-semiconductor and/or a field effect transistor that meet specific performance criteria through the selection of the appropriate semiconductor material(s), doping, and device dimensions.

Unit I **8L**

Review of Electronics in Solids. Electronics in Semiconductors: Introduction, band structure of semiconductors, holes in semiconductors, band structures of some semiconductors, mobile carriers, doping, carriers in doped semiconductors. **Carrier Dynamics in Semiconductors**: Introduction, scattering in semiconductors, velocity electric field relations in semiconductors, very high field transport, carrier transport by diffusion, charge injection and quasi Fermi levels, carrier generation and recombination, continuity equation.

Learning Outcomes:

After completion of this unit the student will be able to

- identify Crystal structure of solids and space lattices (L1).
- solve Schrodinger's wave equation describing the behavior of waves (L1).
- discover Fermi level position using Fermi-Dirac and Maxwell-Boltzmann PDF (L3).
- contrast carrier transport and break down phenomena (L2).
- measure excess carriers density due to charge injection in semiconductors (L3).

Unit II **8L**

Junctions in Semiconductors: Device demands, unbiased p-n junction, p-n junction under bias, real diode, high voltage effects in diodes, modulation and switching ac response. SPICE model**.** **Semiconductor Junctions with metal and insulators:** Metals as conductors, Schottky barrier diode, Ohmic contacts, insulator-semiconductor junctions.

Learning Outcomes:

After completion of this unit the student will be able to

- depict Carrier distribution and field profile at a p-n junction (L2).
- compare Operation p-n junction diode under different bias conditions (L1).
- estimate diode I-V characteristics and non-idealities (L2).
- apply Small signal equivalent model of diode (L3).
- compare Semiconductor junctions with metals and insulators (L1).

Unit III **8L**

Bipolar Junction Transistors: Introduction, Bipolar transistor, static characteristics of bipolar transistors, BJT static performance parameters, secondary effects in real devices, a charge control analysis, bipolar transistor as an inverter, high frequency behavior of BJT. Spice model. Bipolar transistors: A Technology roadmap.

Learning Outcomes:

After completion of this unit the student will be able to

- explain working of BJT (L1).
- distinguish different modes of operation of BJT (L1).
- estimate Static performance parameters (L2).
- construct Hetero structures to improve efficiency (L3).

Unit IV **8L**

Field Effect Transistors(MOSFET): Introduction, MOSFET, structure and fabrication, metal-oxide semiconductor capacitor, capacitance voltage characteristics of the MOS structure, metal oxide semiconductor field effect transistor, important issues in real MOSFETs

Learning Outcomes:

After completion of this unit the student will be able to

1. deduce MOS capacitor model (L1).
2. interpret C-V characteristics of MOS capacitor (L1).
3. explain the physical structure and detailed operation of MOSFETs (L2).
4. find the terminal I-V characteristics of MOSFETs and their associated non-idealities (L2).
5. identify short and long channel effects of MOSFETs (L3).

Unit V **10L**

Field Effect Transistors (JFET, MESFET): Introduction, JFET, MESFET, current voltage characteristics, effects in real devices, high frequency high speed issues. **Semiconductor Optoelectronics:** Introduction, optical absorption in a semiconductor, photo current in a p-n diode, P-I-N photodetector, light emission, semiconductor laser-basic principles.

Learning Outcomes:

After completion of this unit the student will be able to

1. categorize various FETs (L1).
2. compare working of JFET and MESFET (L1).
3. differentiate between JFET and MESFET Effects (L2).
4. discuss high frequency, high speed issues (L3).
5. tell the physical operation of devices like LEDs, lasers and light detectors (L1).

Text Books

1. Jasprit Singh, Semiconductor Devices, Basic Principles, Wiley Student Edition, 2012
2. Ben G. Streetman, Solid State Electronic Devices, 6/e, Prentice Hall India, 2013.

References

1. Yuan Taur, Tak.H.Ning, Fundamentals of Modern VLSI Devices, 2/e, Cambridge University Press, 2011.
2. Donald Neamen, Semiconductors Physics and Devices, Tata McGraw Hill, 2011.
3. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley Publications, 2010.

Course Outcomes:

After successful completion of the course, the student will be able to

1. utilize semiconductor models to analyze carrier densities and carrier transport (L2).
2. understand and utilize the basic governing equations to analyze semiconductor devices (L1).
3. understand and analyze the inner working of semiconductor p-n diodes, Schottky barrier diodes and new semiconductor devices such as JFET, MOSFET(L2).
4. predict the behavior of different optoelectronic devices (L1).

19EEC761: VLSI DSP ARCHITECTURES

L T P C
3 0 0 3

This course introduces the student, DSP Architectures and implementation of digital signal processing algorithms on DSP processors. Digital signal processing is an enabling technology for many applications such as video, speech, wired and wireless communications, and multimedia. The focus of this course will be on design methodologies for realization of dedicated VLSI systems for signal processing applications.

Course Objectives

- To familiarize various DSP algorithms and Pipelining and Parallel Processing in DSP Processors.
- To introduce the concepts of Retiming, Folding and Unfolding
- To impart knowledge about Systolic Architecture Design
- To provide an understanding about Bit Level Arithmetic Architectures and Cord algorithm

Unit I **8L**

Introduction to DSP Systems: Typical DSP algorithms, representation of DSP algorithms, **Iteration Bound:**
Introduction, data flow graph representations, loop bound and Iteration bound. **Pipelining and Parallel Processing:** Introduction, pipelining of fir digital filters, parallel processing, pipelining and parallel processing for low power.

Learning Outcomes:
After completion of this unit the student will be able to

- understand various DSP Algorithms (L1).
- explain about data flow representations(L2).
- describe about operations like Pipelining and Parallel Processing in DSP systems(L1).

Unit II **8L**

Retiming: Introduction, definition and properties, solving systems of inequalities, retiming techniques. **Unfolding:** Introduction, an algorithm for unfolding, properties of unfolding, critical path. applications of unfolding.

Learning Outcomes:
After completion of this unit the student will be able to

- define properties and different retiming techniques (L1).
- explain algorithm and properties of unfolding (L2).
- analyze applications of unfolding (L4).

Unit III **8L**

Folding: Introduction, folding transformation, register minimization techniques, register minimization in folded architectures. **Systolic Architecture Design:** Introduction, systolic array design methodology, FIR systolic arrays, selection of scheduling vector, matrix-matrix multiplication and 2-D systolic array design.

Learning Outcomes:

After completion of this unit the student will be able to

- understand folding and register minimization techniques (L1).
- describe systolic array design methodology (L1).
- discuss about matrix-matrix multiplication and 2D systolic array design (L2).

Unit IV **8L**

Bit-Level Arithmetic Architectures: Introduction, parallel multipliers, bit serial multipliers, bit serial filter design and implementation, canonic signed digit representation, distributed arithmetic.

Learning Outcomes:

After completion of this unit the student will be able to

- Describe bit-level arithmetic architecture of parallel and serial multipliers (L1).
- Explain Canonic signed digit representation (L2).
- Discuss about distributed arithmetic (L2).

Unit V **8L**

CORDIC Algorithm: Introduction to CORDIC algorithm, CORDIC and vector rotation, applications of CORDIC. Redundant Arithmetic: Redundant Number representations, Carry-free radix-2 addition and subtraction.

Learning Outcomes:

After completion of this unit the student will be able to

- Understand CORDIC algorithm (L1).
- Explain applications of CORDIC (L2).
- Implement carry free radix-2 addition and subtraction using CORDIC (L3).

Text Book

1. Keshab Parhi, VLSI Digital Signal Processing, Wiley Student Edition, India, 2010.

References

1. Lan Wanhammer, DSP Integrated Circuits, Elsevier Publications, 2012.
2. George A, Constantinides, Peter Y,K, Cheung, Wayne Luk, Synthesis and Optimization of DSP Algorithms, Kluwer Academic Publishers, 2010.
   Proakis J. Gard and D. G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 4/e, PHI, 2011.

Course Outcomes:

After Successful completion of the course, the student will be able to

- Describe about various DSP Algorithms and Pipelining and Parallel Processing (L1).
- Explain about Retiming, Folding and Unfolding techniques in VLSI DSP Architectures (L2).
- Discuss about Bit Level Arithmetic Architecture (L2).
- Implement CORDIC Algorithm in applications related to VLSI DSP Architectures (L3).

19EEC763: ACTIVE FILTER DESIGN

L T P C
3 0 0 3

This course introduces the student, to the filter design using active components in integrated circuits. The first unit cover basics of operational amplifiers and first order filters. The second explains second order filters. The third unit covers design of different low-pass filter and filter transformations. The fourth unit covers design of filters using LC elements. The last unis covers design of filters using transconductance-C and switched capacitor circuits.

Course Objectives:

- To understand basics of operational amplifier circuits.
- To understand the basics of different filter properties.
- To understand different types of filters based on pass band frequencies.
- To study and analyze first and second order filters.
- To design and analyze filters using LC elements.
- To design and analyze active filters.

Unit I **(8L)**

Operational Amplifiers: Operational amplifier models, opamp slew rate, operational amplifier with resistive feedback, analyzing opamp circuits, examples. **First Order Filters:** Bilinear transfer function and its parts, realization with passive elements, bode plots, active realizations, effect of A(s), cascade design.

Learning Outcomes:

After completion of this unit the student will be able to

- understand different operational amplifier circuits (L1).
- understand the basics of the first order filters (L2).
- understand the design of first order filters (L4).

Unit II **(8L)**

Second Order LowPass and BandPass Filters: Design parameters Q and w_0, second order circuit, frequency response of lowpass and bandpass circuits, integrators, other biquads. **Second Order Filters with Arbitrary transmission zeros:** Summing, voltage feedforward, cascade design revisited.

Learning Outcomes:

After completion of this unit the student will be able to

- understand different second order filter parameters (L2).
- understand different types of filters (L3).
- design different second order filters (L4).

Unit III **(8L)**

Low Pass filters with maximally flat magnitude: Ideal low pass filter, Butterworth response, Butterworth pole locations, low pass filter specifications, arbitrary transmission zeros. **Low Pass filters with Equal Ripple Magnitude Response:** The Chebyshev polynomial, Chebyshev magnitude response, local of Chebyshev poles, comparision of maximally flat and equal ripple responses, Chebyshev filter design. **Frequency Transformation:**

Low pass to highpass, low pass to bandpass, low pass to bandstop, lowpass to multiple passband transformation.

Learning Outcomes:

After completion of this unit the student will be able to

- design and understand butterworth filters (L3).
- design and understand Chebyshev filters (L3).
- understand the frequency transformation in filters (L4).

Unit IV **(8L)**

LC Ladder Filters: Some properties of lossless ladders, a synthesis strategy, General ladder design methods, frequency transformation, **Ladder Simulations by Element Replacement:** The general impedance converter, optimal design of the gic, realizing simple ladders, gorski-popiel embedding technique, bruton'sfdnr technique, creating negative components.

Learning Outcomes:

After completion of this unit the student will be able to

- understand properties of LC ladder filters (L2).
- understand different LC Ladder filters (L2).
- design and analyze ladder filters (L5).

Unit V **(8L)**

Transconductance-C filters: Transconductance cells, elementary transconductance building blocks, first order and second order filters, higher order filters. **Switched Capacitor Filters:** The MOS Switch, the switched capacitor, first order building blocks, second order sections, sampled data operation, switched capacitor first order and second order sections, bilinear transformation, design of switched capacitor cascade filters.

Learning Outcomes:

After completion of this unit the student will be able to

- design first and second order filters using transconductance-C filters (L5).
- know the building blocks used in switched capacitor filter (L3).
- design and analyse filters using switched capacitor circuits (L5).

Text Book

1. Rolf Schaumann, Van Valkenburg, Design of Analog Filters, Oxford University Press, 2010

References

1. Integrated Continuous Time Filters, YannisTsividis and Johannes Voorman, IEEE Press, 2011
2. Design of Analog Filters: Passive, Active RC and Switched Capacitor, Rolf Schaumann, M.S. Ghausi, Kenneth R. Laker, 2010 **Course Outcomes:**

After Successful completion of the course, the student will be able to explain different properties of filters (L1).

- understand different types of filters based on pass band frequencies (L2).
- understand different types of filters based on the transition band (L3).
- design different filters using active and passive components (L5).
- convert one type of filter into other filter using frequency transformation (L4).

19EMC741: RESEARCH METHODOLOGY AND IPR

L T P C
2 0 0 2

This course introduces the student, to the fundamentals of research, research process, technical writing and intellectual property rights. Students will be able to use this knowledge to gain interest in their subject area and pursue their career in research.

Course Objectives:

- To familiarize the meaning, objectives and sources of research
- To acquaint the student with the importance and methods of literature review/research ethics
- To impart the knowledge of technical writing for preparing reports, presentations, research proposals, conference/journal publications
- To introduce the terminology and process of obtaining intellectual property rights
- To expose the intricacies in the process of obtaining patent rights

Unit I **5L**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the meaning of a research problem(L2).
- list the different sources of research problem(L1).
- enumerate the different criteria of good research and list the different errors in selecting research problem(L4).
- contrast the different approaches of research(L3).
- compare the different methods for data collection and analysis(L5).

Unit II **5L**

Effective literature studies approaches, analysis Plagiarism, Research ethics.

Learning Outcomes:

After the completion of this unit, the student will be able to

- list and elaborate the different steps of the research process(L1).
- explain the importance of carrying out an effective literature review (L3).
- identify the research gaps from literature review(L4).
- describe the ethical principles to be following during research process and authorship(L2).
- define the terminology and list the methods to avoid being accused of plagiarism(L2).
- list the different types of research misconduct(L5).

Unit III **5L**

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the attributes, reasons and guidelines for effective technical writing (L3).
- contrast between conference paper, technical presentation and journal paper (L2).
- choose a particular research contribution for patenting or journal publication (L4).
- define the terminology related to citation, citation index, h-index etc (L1).

Unit IV **5L**

Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. **International Scenario**: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the codes and standards in building intellectual property rights(L3).
- list the subject, importance and requirements for of patentability(L5).
- explain the process of patenting and commercialization in academia(L1).
- enumerate the procedure for application preparation, filing and grant of Patents(L2).
- define the terminology related to citation, citation index, h-index etc(L4).

Unit V **8L**

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. **New Developments in IPR**: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Learning Outcomes:

After the completion of this unit, the student will be able to

- explain the scope of patent rights (L1).
- describe the process for licensing and transfer of technology (L3).
- identify the sources of patent information and databases (L2).
- elaborate the administration of patent system (L5).
- describe the new developments in IPR in computer software, biological systems etc (L4).

Text Book(s):

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for Science and engineering students”, Tata Mcgraw Hill India, 2013.
2. Ranjit Kumar, “Research Methodology: A Step by Step Guide for beginners”, 2/e, Prentice Hall of India, 2013.

References:

1. Halbert, “Resisting Intellectual Property”, Taylor and Francis Limited, 2007.
2. Mayall, “Industrial Design”, McGraw Hill, 1992.
3. Niebel, “Product Design”, McGraw Hill, 1974.
4. Asimov, “Introduction to Design”, Prentice Hall, 1962.
5. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016
6. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand Publishers, 2008

Course Outcomes:

After successful completion of the course, the student will be able to

- define the meaning, sources, approaches for research problems (L2).
- explain the guidelines for carrying out effective literature review and identify research gaps (L1).
- describe effective guidelines for preparing technical reports, research publications, presentations and research proposals (L4).
- describe the codes, standards and process of obtaining intellectual property rights (L3).
- enumerate the new developments of IPR in engineering systems (L4).

19EEC725: VLSI CIRCUIT DESIGN LABORATORY

L T P C
0 0 4 2

This course introduces the student, to familiarize the EDA tools, the Characteristics of various Electronics devices, and Digital and Analog Integrated Circuits.

Course Objectives

- To Understand the EDA tools
- To describe and analyze the characteristics of various components (like diode, MOSFETs) with different analysis (like DC, AC, TRANSISANT Analysis etc.)
- To design and estimate various characteristics of digital integrated circuits To design and analyze the various analog circuits.
- To Draw the layout of various schematics

Session – I: Digital IC Design Laboratory

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/SPICE Tools

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)
2. Modeling of Diodes, MOS transistors, Bipolar Transistors etc using SPICE,
3. An Overview of Tanner EDA Tool/MicroWind/Electric/ Magic/LTSpice
4. I-V Curves of NMOS and PMOS Transistors
5. DC Characteristics of CMOS Inverters (VTC, Noise Margin)
6. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)
7. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits
8. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits
9. High Speed and Low Power Design of CMOS Circuits

Session-II: Analog IC Design Laboratory

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence Tools

1. Study of MOS Characteristics and Characterization
2. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)
3. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)
4. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)
5. Design and Simulation of Basic Current Mirror, Cascode Current Mirror
6. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier
7. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

Course Outcomes:

After completion of this Lab, the student will be able to

- familiar with various EDA Tools (L1).
- understand the characteristics of various electronic components (L1).
- design and Analyze the characteristics of digital integrated circuits (L2).
- design and Analyze the frequency response of analog integrated circuits(L2).
- design current sources and current mirrors (L2).
- draw the layout of different schematics. (L3).

19EEC727: FPGA DESIGN LABORATORY

L T P C
0 0 4 2

This course introduces the student, to the fundamental design and description of digital systems like combinational circuits, sequential circuits, memories and Finite Sate Machines(FSM)

Course Objectives:

- To Understand the various modeling styles in Hardware Description Language.
- To describe and analyze the various digital systems (like combinational, sequential, memories and FSM).
- To understand the FPGA architecture and implementation of described circuits into FPGA

Modeling and Functional Simulation and Implementation of the following digital circuits (with Xilinx Vivado tools using VHDL/Verilog Hardware Description Languages and Xilinx/Altera FPGA boards

Part – I Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

Part – II Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder,

Part – III Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs, Implementation of UART/Mini Processors on FPGA/CPLD

Course Outcomes:

After completion of this Lab, the student will be able to

- familiar with various modeling styles in Hardware Description Language and Xilinx Vivado (L1).
- design, Describe and Analyze the combinational circuits (L2).
- design, Describe and Analyze the sequential circuits (L2).
- design, Describe and Analyze memories (L2).
- design, Describe and Analyze FSM (L3).
- implement the described circuits into FPGA (L4).

19EAC741: ENGLISH FOR RESEARCH PAPER WRITING

L T P C
2 0 0 0

This course introduces the student, to the different aspects of research paper writing including planning, preparation, layout, literature review write-up etc. Specifically, the perspective and style of writing in different sections of a research paper is highlighted. Students will have exposed to English language skills relevant to research paper writing.

Course Objectives:

- To write clearly, concisely and carefully by keeping the structure of the paper in mind.
- To use standard phrases in English and further improve his command over it.
- To write with no redundancy, no ambiguity and increase the readability of the paper.
- To plan and organize his paper by following a logical buildup towards a proper conclusion.
- To decide what to include in various parts of the paper.
- To write a suitable title and an abstract in order to attract the attention of the reader.
- To identify the correct style and correct tense.
- To retain the scientific value of the paper by using minimum number of words.

Unit I **5L**

Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Learning Outcomes:

After the completion of this unit, the student will be able to

- to know the expectations of various journals and referees(L2).
- to know the typical structure of a paper(L1).
- learn to put words in a sentence in the correct order (L4).
- to write short and clear sentences from the very beginning of the paper(L5).
- to increase the readability of the paper by making it easy to read and 100% clear(L3).
- learn to be concise without losing any important content(L5).
- to avoid some typical grammar mistakes made in research papers(L1).

Unit II **5L**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

Learning Outcomes:

After the completion of this unit, the student will be able to

- learn to make useful contribution worth recommending for publication (L1).
- learn good use of language to make readers notice the key findings (L3).
- learn to anticipate or predict possible objections to the claims made in the paper(L5).

- to understand what is plagiarism, and how to paraphrase other people's work (L2). learn to attract the right kind of readers with a suitable title(L4).
- learn to sell the abstract to potential readers by attracting their curiosity (L4).

Unit III **6L**

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Learning Outcomes:

After the completion of this unit, the student will be able to

- have a deep knowledge about everything that has been previously written on the topic and decide what is important to know in Introduction(L2).
- learn to provide the right amount of literature regarding the sequence of events leading up to the current situation in the Literature review(L1).

Unit IV

6L

Writing Skills: skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

Learning Outcomes:

After the completion of this unit, the student will be able to

- learn to describe the materials used in experiments and/or the methods used to carry out the research (L1).
- the key skill is in reporting the results simply and clearly (L2).
- learn to structure the Discussion and satisfy the typical requirements of the referees (L1).
- learn to provide a clear and high-impact take-home message in the conclusion (L4).

Unit V

6L

Good Paper Writing: Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

Learning Outcomes:

After the completion of this unit, the student will be able to

- learn various lists of frequently used phrases that have a general acceptance in all disciplines and use in specific sections of the paper (L1).
- learn various kinds of things one should look for when doing the final check (L2).

Text Book (s):

1. Goldbort R, Writing for Science, Yale University Press, 2006
2. Day R, How to Write and Publish a Scientific Paper, Cambridge University Press, 2006 3. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM, Highman, 1998.

References:

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Course Outcomes:

By the end of the course the students will be able to:

- frame the structure of the paper precisely (L2).
- improve his command over English by using standard phrase (L3).
- avoid repetition and mistakes in the paper and increase its readability (L3).
- organize the paper logically towards a proper conclusion (L4).
- decide on the content to be included in various parts of the paper (L5).
- identify whether to use personal or impersonal style in the paper (L5).
- express the content in a clear and concise way (L5).
- attract the attention of the reader by providing a suitable title and an appropriate abstract (L5).

19EAC742: DISASTER MANAGEMENT

L T P C
2 0 0 0

This course is intended to provide fundamental understanding of different aspects of Disaster Management. It will expose the students to the concept and functions of Disaster Management and to build competencies of Disaster Management professionals and development practitioners for effective supporting environment as put by the government in legislative manner. It would also provide basic knowledge, skills pertaining to Planning, Organizing and Decision-making process for Disaster Risk Reduction.

Course Objectives:

- To provide students an exposure to disasters, their significance, types & Comprehensive understanding on the concurrence of Disasters and its management.
- To ensure that students begin to understand the relationship between vulnerability, disasters, disaster prevention, risk reduction and the basic understanding of the research methodology for risk reduction measures.
- Equipped with knowledge, concepts, and principles, skills pertaining to Planning, Organizing, Decisionmaking and Problem solving methods for Disaster Management.
- To develop rudimentary ability to respond to their surroundings with potential disaster response in areas where they live, with due sensitivity.

Unit I

5L

Introduction Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Learning Outcomes
After the completion of this unit, the student will be able to

- define the meaning, list the factors and mention the significance of disaster (L3).
- distinguish between hazard and disaster (L2).
- compare manmade and natural disaster (L4).
- list the types of disaster and describe their magnitude (L1).

Unit II

5L

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the meaning, list the factors and mention the significance of disaster (L2).

- distinguish between hazard and disaster (L1).
- compare manmade and natural disaster (L3).
- list the types of disaster and describe their magnitude (L4).

Unit III

6L

Disaster Prone Areas in India Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the seismic zones and their characteristics (L1).
- identify the areas prone to floods and droughts (L3).
- distinguish between landslides and avalanches (L2).
- identify areas prone to cyclonic and costal hazards (L5).
- enumerate the post disaster diseases and epidemics (L3).

Unit IV

6L

Disaster Preparedness and Management Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, media reports: governmental and Community Preparedness.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the monitoring of phenomena triggering a disaster/hazard (L1).
- evaluate the risk with the use of remote sensing and meteorological data (L5).
- list the governmental and community measures for disaster preparedness (L2).

Unit V

6L

Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define and list the elements of disaster risk (L2).
- enumerate the measures for risk reduction (L3). □ apply the techniques of risk assessment (L1).
- identify the means of people's participation in risk assessment (L5).

Text Book(s):

1. R. Nishith, Singh A.K., Disaster Management in India: Perspectives, issues and strategies, New Royal Book Company., 2008.
2. Sahni, Pardeep, Disaster Mitigation Experiences and Reflections, Prentice Hall of India, New Delhi., 2012
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep and Deep Publication, 2007.

Course Outcomes:

At the end of the course, student will be able to

- identify management activities in pre, during and post phases of disasters (L2).
- plan disaster management activities and specify measure for risk reduction (L1).
- apply risk assessment techniques in real life disaster scenarios (L4).

19EAC743: SANSKRIT FOR TECHNICAL KNOWLEDGE

L T P C
2 0 0 0

This course is intended to expose the student to the fundamentals of Sanskrit language and its technical utility in forming the core principles of many engineering branches. Students taking this course shall be able to relate the core principles of engineering branches to semantics of Sanskrit language

Course Objectives:

- to provide the knowledge of Sanskrit alphabets
- to expose the students to the basic grammar and sentence formation in past/present/future tenses
- to provide a classification of Sanskrit literature and its associated roots
- to demonstrate the relation of core engineering principles to the roots of Sanskrit literature

Unit I **9L**

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define and list the elements of disaster risk(L1).
- enumerate the measures for risk reduction(L2).
- apply the techniques of risk assessment(L4).

Unit II **9L**

Order, Introduction of roots, Technical information about Sanskrit Literature.

Learning Outcomes

After the completion of this unit, the student will be able to

- classify the different branches of Sanskrit literature(L1).
- describe the order and roots of Sanskrit literature(L2).
- relate the applicability of Sanskrit literature to technical principles(L5).

Unit III **9L**

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Learning Outcomes

After the completion of this unit, the student will be able to

- relate the technical concepts of engineering to principles of electrical technology(L1).
- relate the technical concepts of engineering to principles of mechanical engineering(L4).
- apply the use of Sanskrit knowledge to describe the mathematical principles(L3).

Text Book(s):

1. Dr.Vishwas, Abhyaspustakam, Samskrita Bharti Publication, New Delhi, 2005.
2. Vempati Kutumb Shastri, Teach Yourself Sanskrit, Prathama Deeksha, Rashtriya Sanskrit Sansthanam, New Delhi Publication, 2003.
3. Suresh Soni, India's Glorious Scientific Tradition, Ocean books, New Delhi, 2011.

Course Outcomes:

After successful completion of the course, the student will be able to

- get a working knowledge in illustrious Sanskrit, the scientific language in the world (L2).
- get a Learning of Sanskrit to improve brain functioning (L1).
- develop the logic in mathematics, science & other subjects with principles of Sanskrit(L4).
- explore the huge knowledge from ancient literature with the help of Sanskrit (L5).

19EAC744: VALUE EDUCATION

L T P C
2 0 0 0

This course is intended to expose the student to the need for human values and methods to cultivate them for leading an ethical life with good moral conduct. Students taking this course will be able to experience a change in personal and professional behavior with these ethical principles guiding him throughout life

Course Objectives:

- To expose the student to need for values, ethics, self-development and standards
- To make the student understand the meaning of different values including duty, devotion, self-reliance etc.
- To imbibe the different behavioral competencies in students for leading an ethical and happy life
- To expose the student to different characteristic attributes and competencies for leading a successful, ethical and happy profession life.

Unit I

7L

Values and self-development –social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the social values and individual attitudes for self-development (L2).
- describe the Indian vision of humanism (L1).
- distinguish between moral and non-moral acts (L3).
- list the standards and value principles for moral conduct (L5).

Unit II

7L

Importance of cultivation of values. Sense of duty. Devotion, self-reliance. Confidence, concentration. Truthfulness, cleanliness. Honesty, humanity. Power of faith, national unity. Patriotism, love for nature, discipline.

Learning Outcomes:

After the completion of this unit, the student will be able to describe the importance of cultivating values (L1).

- list the different traits of self-developed individual (L3).
- explain the need for loving nature/country/humanity (L2).

Unit III

7L

Personality and Behaviour Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the benefits of positivie thinking, integrity and discipline (L2).
- list the different methods for avoiding fault finding, anger (L4).
- explain the methods to overcome suffering, religious intolerance, self-destructive habits (L3).

Unit IV

7L

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the science of reincarnation (L2).
- explain the relation between self-management and good health (L1).
- elaborate the role of different religions in reaching the common goal (L4).
- list the different techniques for mind-control to improve personality and studies (L3).

Text Book(s):

1. Chakroborty S.K., “Values and ethics for organizations: Theory and Practice”, Oxford University Press, 1998.

Course Outcomes:

After successful completion of the course, the student will be able to

- appreciate the need for human values and methods for self-development (L2).
- elaborate the different traits and benefits of a self-developed individual (L1).
- list the different attributes of self-developed individual (L4).
- elaborate the role and scope of books/faith/health/religions in character building and competence development (L3).

19EAC745: CONSTITUTION OF INDIA

L T P C
2 0 0 0

This course is intended to expose the student to the philosophy of Indian constitution. Students will be able to understand their fundamental rights/duties and governance structure. Students also appreciate the role of election commission in establishing a democratic society.

Course Objectives:

- To familiarize the student about the need for a constitution
- To make the student understand the role of constitution in a democratic society
- To acquaint the student with key constitutional features and fundamental rights of a citizen
- To impart the organs of governance and local administration hierarchy and their responsibilities
- To familiarize the student with the role, responsibilities and administration hierarchy of election commission

Unit I

5L History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working). **Philosophy of the Indian Constitution**: Preamble, Salient Features

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the outline of drafting committee and their roles in the making of Indian constitution (L1)
- describe the need and role of a constitution in a democratic society (L1)
- elaborate the salient features of Indian constitution (L2)

Unit II

5L Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the fundamental rights of a citizen (L2)
- explain the intricacies in the different rights (L3)
- elaborate the fundamental duties of a citizen (L3)
- describe the principles of state policy (L4)

Unit III **6L**

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions

Learning Outcomes:

After the completion of this unit, the student will be able to

- present the hierarchy of governance (L3)
- list the role/responsibilities/powers of different organs of governance (L4)
- elaborate the guidelines for appointment/transfer of judges (L5)

Unit IV **6L**

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Panchayat raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Learning Outcomes:
After the completion of this unit, the student will be able to
- describe the administrative organizational hierarchy of municipalities and panchayats(L4)
- appreciate the role/responsibilities/powers of mayor, CEO, elected officials (L5)
- appreciate the importance of grass root democracy (l5)

Unit V **6L**

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Learning Outcomes:
After the completion of this unit, the student will be able to
- describe the administrative hierarchy of election commission (L5)
- elaborate the roles/responsibilities/powers of election commissioners at different levels of hierarchy (L5)
- outline the welfare activities of SC/ST/OBC/Women by different bodies (L4 & L5)

Text Book(s):
1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. S. N. Busi, Dr. B. R. Ambedkar, Framing of Indian Constitution, 1/e, 2015.
3. M. P. Jain, Indian Constitution Law, 7/e, Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes:

After successful completion of the course, the student will be able to
- describe the philosophy and salient features of Indian constitution (L1)
- list the constitutional rights and duties of a citizen (L3)
- elaborate the central and local administrative hierarchy and their roles (L2)
- describe the roles/responsibilities/powers of different governing and administrative bodies (L4)
- explain the structure/functioning and power of election commission (L5)

19EAC746: PEDAGOGY STUDIES

L T P C
2 0 0 0

This course is aimed to familiarizing the student with pedagogical principles, practices and methodologies. This course is intended for students interested in pursuing a career in teaching and research.

Course Objectives:

- To familiarize the student about the need for pedagogy studies, background and conceptual framework
- To expose the student to pedagogical practices in formal/informal classrooms
- To acquaint the student with type of curriculum and guidance materials for effective pedagogy
- To familiarize the student with classroom practices and curriculum assessment procedures
- To make the student understand the effect of undertaking research on teaching quality

Unit I **5L**

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

Learning Outcomes:

After the completion of this unit, the student will
be able to define the aim and rationale behind teacher education (L2).

- classify the different theories of learning (L1).
- elaborate the need and role of curriculum, teacher education (L3).

Unit II **5L**

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the different pedagogical practices used by teachers in formal and informal classrooms(L2).
- explain the pedagogical practices employed in developing countries (L1).
- enumerate the duties of faculty in terms of teaching, research, consultancy, administration (L4).

Unit III **6L**

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change.

Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Learning Outcomes:

After the completion of this unit, the student will be able to list the measures for effective pedagogy (L1).

- identify the different documentation required to formalize curriculum implementation and quality assessment (L3).
- describe the teachers attitudes and beliefs in pedagogic strategies (L4).

Unit IV **6L**

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the organizational hierarchy in a school administration system (L3).
- list the different barriers to learning (L1).
- enumerate the methods to overcome limited resources and handle large class sizes (L4).
- describe the follow-up support and peer-support in classroom practices (L2).

Unit V **6L**

Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Learning Outcomes:

After the completion of this unit, the student will be able to

- explain the need for and role of research in teaching profession (L1).
- list the different research activities to be taken up by teachers (L2).
- describe the impact of research on teaching quality and learning process (L4).

Text Book(s):

1. Ackers J, Hardman F, Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261, 2001 2. Agrawal M, Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36
(3): 361-379, 2004.
3. Akyeampong K, Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID., 2003.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J, Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282., 2013.
5. Alexander RJ, Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell., 2001.
6. Chavan M, Read India: A mass scale, rapid, 'Learning to Read' campaign., 2003.

Course Outcomes:

After successful completion of the course, the student will be able to

- describe the theories of learning and conceptual framework of pedagogy (L2).
- explain the pedagogical practices used by teachers in formal and informal classrooms (L1).
- visualize the administrative hierarchy of schools and colleges and define the role (L4).
- appreciate the need for research and define the future direction of teaching career (L3).
- describe the impact of curriculum and assessment on the teaching learning process of a student (L5).

19EAC747: STRESS MANAGEMENT BY YOGA

L	T	P	C
2	0	0	0

This course is aimed to familiarize the student with basic principles of yoga and different physical/mental practices for managing mind and body. This course helps the student in managing stress during education, home and workplace. Further, principles learnt in this course help in building overall personality for a stress-free, happy and independent life.

Course Objectives:

- To familiarize the student about eight parts of yoga and their significance To expose the student to the importance and meaning of Yam and Niyam
- To make the student understand the meaning and importance of yogic principles including Ahimsa, Satya, Astheya etc
- To introduce the different yogic poses with a knowledge of their benefits for mind and body
- To familiarize the effect of different types of breathing techniques in concept and in activity

Unit I **9L**

Definitions of Eight parts of yoga (Ashtanga).

Learning Outcomes:

After the completion of this unit, the student will be able to
list the eight parts of yoga(L2).
- describe the effects of different parts of yoga on mind and body(L1).
- elaborate the importance of yoga in stress management and personality development(L3).

Unit II **9L**

Yam and Niyam.
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan.

Learning Outcomes:

After the completion of this unit, the student will be able to
elaborate the importance of Yam and Niyam (L2).
- describe the meaning and significance of Ahinsa, satya, astheya etc (L1).
- explain the need for shaucha, santosh, tapa, swadhyay in leading a healthy and fruitful life (L3).

Unit III **9L**

Asan and Pranayam
i) Various yog poses and their benefits for mind & body ii) Regularization of breathing techniques and its Effects-Types of pranayam.

Learning Outcomes:

After the completion of this unit, the student will be able to

1. demonstrate the different physical asanas and explain their physical and phychological effects(L1).
2. demonstrate the different breathing techniques and describe their physical and mental effects (L3).
3. distinguish between different types of pranayamam(L4).

Text Books

1. Janardan, Yogic Asanas for Group Tarining-Part-I, Swami Yogabhyasi Mandal, Nagpur
2. Swami Vivekananda, "Rajayoga or conquering the Internal Nature", Advaita Ashrama, Kolkata

Course Outcomes:

After successful completion of the course, the student will be able to

describe the eight parts of yoga and their significance (L1).

- explain the the importance and meaning of Yam and Niyam (L3).
- define the meaning and importance of yogic principles including Ahimsa, Satya, Astheya etc (L2).
- demonstrate the different yogic poses and explain their benefits for mind and body (L4).
- demonstrate the different types of breathing techniques and explain their physical and mental benefits (L5).

19EAC748: PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

L T P C
2 0 0 0

This course is aimed to familiarize the student with life enlightenment skills for personality development. This course helps the student in building his holistic personality through human values, ethics and spiritual attributes.

Course Objectives:

- To familiarize the student to good personality traits through moral stories
- To make the student understand the goal of human life and importance of good personality in reaching the goal
- To expose the student to the study of Shrimad-Bhagwad-Geeta for developing his/her personality and achieve the highest goal in life
- To familiarize the student to leadership skills for driving nation and mankind to peace and prosperity
- To expose the role of Neetishatakam for developing versatile personality of students.

Unit I **9L**

Neetisatakam-Holistic development of personality
Verses- 19,20,21,22 (wisdom)
Verses- 29,31,32 (pride & heroism)
Verses- 26,28,63,65 (virtue)
Verses- 52,53,59 (dont's)
Verses- 71,73,75,78 (do's).

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the moral stories illustrating the traits of good personality (L1)
- define the meaning and importance of wisdom, pride, heroism, virtue etc (L2)
- identify do and donts in life from the foundations of human morals/ethics (L2)

Unit II **9L**

Approach to day to day work and duties.
Shrimad BhagwadGeeta: Chapter 2-Verses 41, 47,48,
Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, Chapter 18-Verses 45, 46, 48.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the characteristics and principles of bhakti yogam, jnana yogam and karma yogam (L3)

- identify the use of different yogic characteristics in different activities of daily life/duties (L4)
- apply the use of yogic principles for leading a stress-free, happy and fruitful life with good developed personality (L4)

Unit III **9L**

Statements of basic knowledge.
Shrimad BhagwadGeeta: Chapter2-Verses 56, 62, 68
Chapter 12 -Verses 13, 14, 15, 16,17, 18
Personality of Role model. Shrimad BhagwadGeeta:
Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
Chapter 4-Verses 18, 38,39
Chapter18 – Verses 37,38,63

Learning Outcomes:

After the completion of this unit, the student will be able to

1. list the characteristics of role model proposed by verses of bhagavad gita (L3)
2. explain the methods for obtaining life enlightenment through the practice of four yoga appropriately (L4)
3. describe the characteristics of karma yogi/jnana yogi for developing leadership personality (L5)

Text Book(s):

1. Swami Swarupananda, “Srimad Bhagavad Gita”, Advaita Ashram (Publication Department), Kolkata
2. P. Gopinath, Bhartrihari’s Three Satakam (Niti-Sringar-vairagya), Rashtriya Sanskrit Sansthanam, New Delhi.

Course Outcomes:

After successful completion of the course, the student will be able to

- List the different parables of neethisathakam and identify their morals (L1)
- enumerate the different traits of human personality for life enlightenment (L2)
- describe the leadership attributes for driving nation and mankind to peace and prosperity (L3)
- explain the applicability of different types of yoga to day-to-day work and duties resulting in responsible personality (L4)

19EAC750: DEVELOPING SOFT SKILLS AND PERSONALITY

L	T	P	C
2	0	0	0

Soft skills comprise pleasant and appealing personality traits as self-confidence, positive attitude, emotional intelligence, social grace, flexibility, friendliness and effective communication skills. The course aims to cause a basic awareness within the students about the significance of soft skills in professional and inter-personal communications and facilitate an all-round development of personality.

Course Objectives

- To familiarize the student to the criteria for self-assessment and significance of selfdiscipline.
- To expose the student to attitudes, mindsets, values and beliefs.
- To acquaint the student to plan career and goals through constructive thinking.
- To enable the student to overcome barriers for active listening and persuasive speaking.
- To familiarize the skill of conducting meetings, writing minutes and involving in active group discussions.

Unit I **8L**

Self-Assessment; Identifying Strength & Limitations; Habits, Will-Power and Drives; Developing Self-Esteem and Building Self-Confidence, Significance of Self-Discipline

Learning Outcomes

After the completion of this unit, the student will be able to

- identify strengths & limitations through self-assessment(L3)
- list the attributes of personalities will good will-power and self-drives(L1)
- describe the reasons for building self-esteem and self-confidence(L2)
- explain the significance of self-discipline(L2)

Unit II **8L**

Understanding Perceptions, Attitudes, and Personality Types: Mind-Set: Growth and Fixed; Values and Beliefs

Learning Outcomes

After the completion of this unit, the student will be able to

- define the characteristics of different perceptions, attitudes and personality types(L1)
- distinguish between fixed and growing mindsets(L3)
- define the importance and meaning of values and beliefs(L2)

Unit III **8L**

Motivation and Achieving Excellence; Self-Actualisation Need; Goal Setting, Life and Career Planning; Constructive Thinking

Learning Outcomes

After the completion of this unit, the student will be able to

- describe the need for having high motivation and achieving excellence(L2)
- define the need for self-actualization(L1)
- plan the life and career goals based on self assessment(L4)

- explain the attributes of constructive thinking(L2)

Unit IV **8L**

Communicating Clearly: Understanding and Overcoming barriers; Active Listening; Persuasive Speaking and Presentation Skills.

Learning Outcomes

After the completion of this unit, the student will be able to

- self-assess the barriers for communicating clearly (L4)
- list the attributes of active listening(L1)
- describe the minimal aspects of effective presentation(L2)
- organize ideas resulting a persuasive talk(L3)

Unit V **8L**

Conducting Meetings, Writing Minutes, Sending Memos and Notices; Netiquette: Effective Email Communication; Telephone Etiquette; Body Language in Group Discussion and Interview.

Learning Outcomes

After the completion of this unit, the student will be able to

- describe the format and structure of writing meeting minutes(L2)
- identify the essential components of memos and notices(L3)
- explain the principles of effective email communication(L2)
- list the basic etiquette of telephone conversation(L1)
- describe the effective body traits during group discussion and interviews(L2)

Text Books

1. Dorch, Patricia. What Are Soft Skills? New York: Execu Dress Publisher, 2013.
2. Kamin, Maxine. Soft Skills Revolution: A Guide for Connecting with Compassion for Trainers, Teams, and Leaders. Washington, DC: Pfeiffer & Company, 2013.
3. Klaus, Peggy, Jane Rohman& Molly Hamaker. The Hard Truth about Soft Skills. London: HarperCollins E-books, 2007.
4. Petes S. J., Francis. Soft Skills and Professional Communication. New Delhi: Tata McGraw-Hill Education, 2011.
5. Stein, Steven J. & Howard E. Book. The EQ Edge: Emotional Intelligence and Your Success. Canada: Wiley & Sons, 2006.

Course Outcomes

After successful completion of the course, the student will be able to

- carry out self-assessment and describe the significance of self-discipline(L4)
- define, classify and compare attitudes, mindsets, values and beliefs(L3)
- plan career and goals through constructive thinking and personal assessment(L4)
- overcome barriers for active listening and persuasive speaking (L5)
- conduct meetings, write minutes and involve in active group discussions(L3)

19EEC706: VLSI TECHNOLOGY

L	T	P	C
3	0	0	3

This course introduces to the student, to understand the fundamental concepts of VLSI fabrication, and the kinetics and quality measures involved in each fabrication stage. This subject provides basic knowledge required for both electrical and electronics students to understand forthcoming subjects in the VLSI Design specialization, and gives ample knowledge to work in the semiconductor fabrication industry.

Course objectives:

- To understand the semiconductor materials, devices and technology historical evaluations
- To explain the oxidization process and quality measures in the fabrication
- To explain lithography importance in the semiconductor industry and the various techniques
- To understand other process steps like etching, implantation and metallization and their implications.
- To explain the passive components fabrication process
- To understand the impact of other semiconductor technologies like MEMS To understand the concepts of electrical testing and packaging of ICs

Unit I **8L**

Introduction: Semiconductor materials, semiconductor devices, semiconductor process technology, basic fabrication steps. **Crystal growth**: Silicon crystal growth from melt, silicon float-zone process, GaAs crystal growth techniques, material characterization.

Learning outcomes:

After completion of this unit the student will be able to

- understand t different semiconductor materials and devices (L2).
- understands fabrication process flow (L2).
- understands the single crystal development process and the process parameters (L2).
- explains the temperature ranges of single crystal techniques (L4).

Unit II **8L**

Silicon Oxidation: Thermal oxidation, impurity redistribution during oxidation, masking properties of silicon dioxide, oxide quality, oxide thickness characterization. **Photolithography**: Optical lithography, E-beam lithography.

Learning outcomes:

After completion of this unit the student will be able to

- explain the oxidization process and techniques (L3).
- analyse the kinetics of oxidization process (L4).
- know the process of oxide quality tests (L2).
- understand the lithography importance and various lithographic techniques (L2).

Unit III **8L**

Etching: Wet chemical etching, Dry etching. **Diffusion**: Basic diffusion process, extrinsic diffusion, laterals diffusion.

Learning outcomes:

After completion of this unit the student will be able to

- understand the basic chemical etching process (L2).
- analyze the etch parameters and etch rates (L4).
- apply the etching process for different materials (L3).
- understand the process and differences of diffusion (L2). □ deduce the lateral diffusion parameters (L5).

Unit IV **8L**

Ion Implantation: Range of implanted ions, implant damage and annealing. **Film Deposition**: Epitaxial growth techniques, structures and defects in epitaxial layers, dielectric deposition, polysilicon deposition.

Learning outcomes:

After completion of this unit the student will be able to

- understand the ion implantation process in the fabrication (L2).
- understand the annealing and implant damages in the ion implantation process (L2).
- analyze defects and range of defects in the implantation process (L4).
- apply the concept of film deposition to polysilicon and metal deposition (L3).

Unit V **10L**

Process Integration: Passive components, bipolar technology, MESFET technology, MEMS technology. **IC Manufacturing**: Electrical testing, Packaging.

Learning outcomes:

After completion of this unit the student will be able to

- learn the passive devices fabrication (L1).
- understand various fabrication technologies (L2).
- analyze the electrical test procedures and benefits (L4).
- understand the IC packaging methods (L2).

Text Book

1. Gary S May & Simon M Sze, Fundamentals of Semiconductor Fabrication, Wiley Student Edition, 2012.

References

1. S. K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc, 2010.
2. S. M. Sze, VLSI Technology, 2/e, McGraw Hill, 2011.
3. Stephen Cambell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2013.

Course Outcomes:

After successful completion of the course, the student will be able to

- know the new semiconductor materials and VLSI fabrication flow (L1).
- explain the process of oxide coating in the fabrication industry and measurement of qualities (L2).
- explain the lithography procedure and advanced lithography techniques using in the industry (L3).
- apply the knowledge lithography in metallization and epi growth (L4).
- understand the different IC technologies, electrical testing and packaging process of VLSI chips (L5).

19EEC760: RF IC DESIGN

L	T	P	C
3	0	0	3

This course introduces the student, to the fundamental principles and building blocks of radio frequency integrated circuits. The student learns the design and implementation of RF transceivers, low noise amplifiers, mixers, phase locked loops and frequency synthesizers. Students will be able to use this knowledge in the design of Bluetooth, WiFi, GSM, 3G, 4G, 5G transceivers as per relevant standards.

Course Objectives:

- To familiarize the basic concepts in RF design on the characterization of nonlinearity, noise, scattering parameters.
- To acquaint the student will knowledge of wireless standards and their specifications
- To impart the knowledge of different transceiver architectures and their tradeoffs
- To introduce the design of low noise amplifiers, mixers and passive devices
- To expose the design issues in oscillators, frequency synthesizers and RF power amplifiers

Unit I **8L**

Basic Concepts in RF Design: General considerations, effects of nonlinearity, noise, sensitivity and dynamic range, passive impedance transformation, scattering parameters. **Communication Concepts**: General considerations, analog modulation, digital modulation, spectral regrowth, multiple access techniques, wireless standards

Learning Outcomes:

After the completion of this unit, the student will be able to

- define and compute the various parameters characterizing the nonlinearity including gain compression, intermodulation and harmonic distortion (L1).
- characterize a given receiver circuit by its noise figure, sensitivity and dynamic range (L2).
- design input and output matching networks for impedance transformation (L4).
- enumerate the different specifications of a wireless standard (L1).

Unit II **8L**

Transceiver Architectures: General considerations, receiver architectures, transmitter architectures, OOK transceivers.

Learning Outcomes:

After the completion of this unit, the student will be able to

- enumerate the different requirements of RF receivers including bandwidth, channel selection, band selection and Tx-Rx feedthrough (L2).
- define and compare the basic principles of heterodyne, direct-conversion and low-IF receiver architectures (L3).
- describe and compare the different RF transmitter architectures and their tradeoffs (L5).

Unit III **8L**

Low-Noise Amplifiers: General considerations, problem of input matching, LNA topologies, gain switching, band switching.

Learning Outcomes:

After the completion of this unit, the student will be able to

- enumerate the different requirements of low noise amplifiers including noise figure, gain, input return loss, stability, linearity and bandwidth (L1).
- describe the problem of input matching in low noise amplifiers (L2).
- analyze the design tradeoffs in different LNA topologies including CS stage with inductive load, CG stage, Cascode stage with inductive degeneration (L5).
- describe the implementation of band switching and gain switching in low noise amplifier topologies (L3).

Unit IV **8L**

Mixers: General considerations, passive down conversion mixers, active down conversion mixers, upconversion mixers. **Passive Devices:** General considerations, inductors, transformers, transmission lines, varactors, constant capacitors.

Learning Outcomes:

After the completion of this unit, the student will be able to

- enumerate the performance parameters of mixers including noise figure, linearity and portto-port feedthrough (L1).
- explain the operation and design of single balanced and double balanced mixers with neat sketches (L4).
- compare the design tradeoffs in passive and active down conversion mixers (L5).

Unit V **8L**

Oscillators: Performance parameters, basic principles, cross-coupled oscillator, three-point oscillators, voltage-controlled oscillators, LC VCOs with wide tuning range, phase noise, design procedure, low-noise VCOs, LO interface, mathematical model of VCOs. **Phase-Locked Loops:** Basic concepts, type-I PLLs, type-II PLLs, PFD/CP non idealities, Phase noise in PLLs, loop bandwidth, design procedure, overview of integer and fractional frequency synthesizers, power amplifiers, transceiver design example.

Learning Outcomes:

After the completion of this unit, the student will be able to

- enumerate the performance parameters of oscillators including frequency range, output voltage swing, drive capability, phase noise, supply sensitivity and tuning range (L1).
- explain the operation and design tradeoffs in cross-coupled oscillators (L4).

- list the basic concepts of voltage controlled oscillators and implementation of tunability is oscillator circuits (L1).
- explain the operation of Type-I and type-II PLLs and compare their design tradeoffs (L3).

Text Book

1. Behzad Razavi, RF Microelectronics, 2/e, Pearson Education, 2011.

References

1. Leung Bosco, VLSI for Wireless Communication, 2/e, Springer 2011.
2. Thomas Lee, Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press, 2013.

Course Outcomes:

After successful completion of the course, the student will be able to

- describe the computation of RF parameters including P1dB, IIP3, noise figure and scattering parameters (L2).
- list and describe the different specifications of wireless standards and derive specifications for individual building blocks (L1).
- compare and identify a suitable transceiver architecture for given transceiver specifications (L4).
- analyze and design low noise amplifiers, mixers and passive devices for given specifications (L4).
- explain the principles and operation of oscillators, frequency synthesizers and RF power amplifiers (L2).

19EEC762: ADVANCED LOGIC SYNTHESIS

L	T	P	C
3	0	0	3

This course introduces the student, to Synthesis flow, coding related to synthesis, setting the environment & logical libraries, setting synthesis constraints, perform synthesis using EDA tools, analyzing the synthesis reports Principles of RTL Design, optimization of design. Moreover, logic synthesis makes it possible to re-target a given design to new and emerging semiconductor technologies.

Course Objectives:

- To learn High-Level Design Methodology and overview of design flow To learn the coding skills relevant to synthesis of logic circuits.
- To understand importance of libraries in synthesis flow
- To design logic to meet specifications and optimization
- To understand the design constrains related to FSM

Unit I **8L**

High-Level Design Methodology Overview: ASIC Design Flow Using Synthesis, HDL Coding, RTL Behavioral and Gate-Level Simulation, Logic Synthesis, Design for Testability, Design ReUse, Behavioral Synthesis & Concepts. Design Analyzer and Design compiler, Target Library, Link Library, and Symbol Library, Cell names, Instance names, and VHDL Libraries in the Synthesis Environment, Synthesis, Optimization and Compile, Classic Scenarios

Learning Outcomes:

After completion of this unit the student will be able to

- understand the synthesis based ASIC design flow (L1).
- basics related to steps involve in logic synthesis (L2).
- understand the compliers and libraries (L3).
- directly proceed to specific issues (L4).

Unit II **8L**

VHDL/Verilog Coding for Synthesis: General HDL Coding Issues, VHDL vs. Verilog: The Language Issue, Finite State Machines, HDL Coding Examples, Classic Scenarios.

Learning Outcomes:

After completion of this unit the student will be able to

- deal with the very first stage in the synthesis process – HDL coding (L1).
- several recommendations for writing synthesizable HDL code(L2).
- coding for finite state machines (L5).
- understand the classical scenarios related to synthesizable coding (L4).

Unit III **8L**

Links to Layout, Motivation for Links to Layout Floor planning, Link to Layout Flow Using Floorplan Manager, Creating Wire Load Models After Back-Annotation Re-Optimizing Designs After P&R. Design for Testability: Introduction to Test Synthesis, Test Synthesis Using Test Compiler

Learning Outcomes:

After completion of this unit the student will be able to

- understand the layout and floor planning (L1).
- learn the back annotation (L2).
- learn the drawing the PR boundaries (L5).
- design the testable circuits (L4).

Unit IV **8L**

Constraining and Optimizing Designs: Synthesis Background, Clock Specification for Synthesis, Design Compiler Timing Reports, Commonly Used Design, Compiler Commands, Strategies for Compiling Designs, Typical Scenarios When Optimizing Designs, Guidelines for Logic Synthesis, Classic Scenarios.

Learning Outcomes:

After completion of this unit the student will be able to

- learn about constraining designs to achieve the optimal design (L1).
- get the best out of the Design Compiler (L5).
- understand synthesis covering optimization constraints (L2).
- learn the guidelines of logic synthesis (L4).

Unit V **8L**

Constraining and Optimizing Designs for FSM: Finite State Machine (FSM) Synthesis, Fixing Min Delay Violations Technology Translation, Translating Designs with Black-Box Cells, Pad Synthesis, Classic Scenarios

Learning Outcomes:

After completion of this unit the student will be able to

- design the FSM related to synthesis (L4).
- learn the delay violation while translation(L3).
- synthesizing of Post synthesis (L3).
- understand the classical scenarios(L5).

Text Book

1. Kurup Pran, Taher Abbasi, Logic Synthesis using Synopsys, 2/e, Pearson Education, 2007.

References

1. VHDL for Logic Synthesis, Third Edition. Andrew Rushton. © 2011 John Wiley & Sons, Ltd. Published 2011 by John Wiley & Sons, Ltd.
2. Weng Fook Lee, VHDL Coding and Logic Synthesis with Synopsys, Academic Press, 2000
3. Morris Mano, Michael D. Ciletti, Digital Design , 4/e, Prentice Hall of India, 2008
4. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis, Springer Science, 2013
5. http: www.nptel.ac.in

Course Outcomes:

After successful completion of the course, the student will be able to

- understand synthesis Flow and optimization (L1).
- understand synthesizable coding concepts (L2).
- analyze physical design concepts (L3).
- understand efficient way of giving constrains (L4).
- analyze constraining and Optimizing Designs for FSM (L5).

19EEC764: ADVANCED DIGITAL IC DESIGN

L	T	P	C
3	0	0	3

This course introduces the student, to advanced topics of integrated circuit designs, implementation strategies of IC design, interconnecting's and its issues, timing concepts of advanced IC designs, building varieties of arithmetic circuit designs, memory designs. these concepts give the full understanding and ability to construct various digital IC designs.

Course Objectives:

- Understand the implementation strategies in IC deign
- Learn estimation of delays in IC design and wires
- Understand the importance of timing and issues related to IC design
- Design logic to meet specifications and optimization
- Learn the construction of arithmetic circuit design
- Learn the Designing Memory and Array Structures

Unit I **8L**

Implementation Strategies for Digital ICs: Introduction, from custom to semicustom and structured array design approaches, custom circuit design, cell-based design methodology, standard cell, compiled cells, macrocells, megacells and intellectual property, semi-custom design flow, array-based implementation approaches, pre-diffused (or mask-programmable) arrays, prewired arrays.

Learning Outcomes:

After completion of this unit the student will be able to

- Determining difference between full custom, semicustom and structure methods (L1).
- Introducing the cell based design (ASIC flow) (L1).
- Understand the semicustom design flow (L2).
- Learn the array based design approaches and pre wired arrays (L3).

Unit II **8L**

The Wire: Introduction, a first glance, interconnect parameters—capacitance, resistance, and inductance, electrical wire models, spice wire models**. Coping with interconnect:** introduction, capacitive parasitic, capacitance and reliability-cross talk, capacitance and performance in CMOS, resistive parasitic, resistance and reliability-ohmic voltage drop, electromigration, resistance and performance—RC delay.

Learning Outcomes:

After completion of this unit the student will be able to

- determining and quantifying interconnect parameters (L1).
- introducing circuit models for interconnect wires (L2).
- driving large capacitors (L3).
- dealing with transmission line effects in wires (L1).
- signal integrity in the presence of interconnect parasitic (L4).

Unit III **8L**

Timing Issues in Digital Circuits: Introduction, timing classification of digital systems, synchronous interconnect, mesochronous interconnect, plesiochronous interconnect, asynchronous interconnect, synchronous design an in-depth perspective, synchronous timing basics, sources of skew and jitter, clock-distribution techniques, synchronizers and arbiters, synchronizers—concept and implementation, arbiters, clock synthesis and synchronization using a phase-locked loop, basic concept, building blocks of a PLL.

Learning Outcomes:

After completion of this unit the student will be able to

- impact of clock skew and jitter on performance and functionality (L1).
- alternative timing methodologies (L2).
- synchronization issues in digital IC and board design (L3).
- clock generation (L4).

Unit IV **8L**

Designing Arithmetic Building Blocks: Introduction, datapaths in digital processor architectures, the adder, the binary adder, definitions, the full adder, circuit design considerations, the binary adder, logic design considerations, the multiplier, the multiplier, definitions, partial-product generation, partial product accumulation, final addition, multiplier summary, the shifter, barrel shifter, logarithmic shifter.

Learning Outcomes:

After completion of this unit the student will be able to

- understand the data path units and control unites for architectures (L2).
- learn designing of various arithmetic circuits (adders, multipliers etc.) (L3).
- learn the design of shifters (L5).

Unit V **8L**

Designing Memory and Array Structures: Introduction, memory classification, memory architectures and building blocks, the memory core, read-only memories, nonvolatile read-write memories, read-write memories (RAM), contents-addressable or associative memory (CAM), memory peripheral circuitry, the address decoders, sense amplifiers, voltage references, drivers/buffers, timing and control.

Learning Outcomes

After completion of this unit the student will be able to

- understand the calcification of memories (L2).
- learn designing of various memories (L3).
- learn the design of sensing amplifiers (L5).
- understand the timing and control unit design (L4).

Text Book

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits – A design perspective, Second Edition, Pearson Education, 2012.

References

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, Third Edition, McGraw Hill, 2012.

2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits, 3rd Ed, TMH Publication, 2010.
3. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2011.

Course Outcomes:

After successful completion of the course, the student will be able to

- understand implementation storages (L1).
- understand wiring concepts (L2).
- analyze timing constrains in digital circuits (L3).
- design arithmetic circuits (L4).
- understand the design of memories and array architectures (L5).

19EEC766: ASIC DESIGN

L	T	P	C
3	0	0	3

Course Description:
This course emphasis the fundamentals principles and design processes used in the design of chips using design automation tools. Specifically, the course highlights algorithmic principles behind logic synthesis, static timing analysis, design for test, placement and routing tools

Course Educational Objectives:

1. To impart the synthesizable aspects of VLSI Constructs
2. To acquaint the students with timing constraints and analysis concepts
3. To elaborate different aspects of Logic Synthesis, Physical Synthesis process
4. To expose the design concerns in chip design signoff and packaging

UNIT 1 Introduction to Chip Design Flow 8 hours

Basic Concepts of Integrated Circuit: Structure, Fabrication, Types, Design Styles, Designing vs. Fabrication, Economics, Figures of Merit Overview of VLSI Design Flow: Design Flows and Abstraction; Pre-RTL Methodologies: Hardware-software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioural Synthesis. Overview of VLSI Design Flow: RTL to GDS Implementation: Logic Synthesis, Physical Design; Verification and Testing; PostGDS Processes

UNIT 2 RTL Design and Synthesis 8 hours

Hardware Modeling: Introduction to Verilog Functional verification using simulation: testbench, coverage, mechanism of simulation in Verilog. RTL Synthesis: Verilog Constructs to Hardware Logic Optimization: Definitions, Two-level logic optimization Logic Optimization: Multi-level logic optimization, FSM Optimization Formal Verification: Introduction, Formal Engines: BDD, SAT Solver Formal Verification: Model Checking, Combinational Equivalence Checking Technology Library: Delay models of Combinational and Sequential Cells

UNIT 3 Static Timing Analysis 8 hours

Static Timing Analysis: Synchronous Behaviour, Timing Requirements, Timing Graph, Mechanism, Delay Calculation, Graph based Analysis, Path-based Analysis, Accounting for Variations. Constraints: Clock, I/O, Timing Exceptions Technology Mapping Timing-driven Optimizations, Power Analysis, Power-driven Optimizations

UNIT 4 Design for Testability 8 hours

Design for Test: Basics and Fault Models, Scan Design Methodology. Design for Test: ATPG, BIST

UNIT 5 Floorplanning, Placement, Routing and Clock Distribution 8 hours

Basic Concepts for Physical Design: IC Fabrication, FEOL, BEOL, Interconnects and Parasitics, Signal Integrity, Antenna Effect, LEF files. Chip Planning: Partitioning, Floorplanning, Power Planning Placement: Global Placement, Wirelength Estimates, Legalization, Detailed Placement, Timing-driven Placement, Scan Cell Reordering, Spare Cell Placement. Clock Tree Synthesis: Terminologies, Clock Distribution Networks, Clock Network Architectures, Useful Skews Routing: Global and Detailed, Optimizations Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off

Textbooks:

1. Sneh Saurabh, Introduction to VLSI Design Flow, Cambridge University Press, 2023.
2. Adam Teman, Digital VLSI Design course https://www.eng.biu.ac.il/temanad/digital-vlsi-design/

References:

1. N.A.Sherwani , “Algorithms for VLSI Physical Design Automation”, (3/e),Kluwer,1999
2. M. Sait , H. Youssef, “VLSI Physical Design Automation”, World scientific, 1999
3. M.Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996
4. Habib Youssef, VLSI Physical Design Automation, World Scientific,2001
5. Sebastian Smith, Application Specific Integrated Circuits, Pearson Education, 2005.
6. Sung Kyu Lim,Practical Problems in VLSI Physical Design, Springer,2008
7. Sabih H Gerez, Algorithms for VLSI Design Automation, Wiley,2006

Course Outcomes:

By the end of the course, the student will be able to

1. Write synthesizable RTL models in standard coding style
2. perform logic synthesis with area/power/delay constraints
3. Perform static timing analysis and fix digital circuits with timing violations
4. Choose appropriate floorplanning, power planning and clock distribution strategies under design constraints
5. Elaborate the design issues for chip finishing and signoff

19EEC768: BROADBAND COMMUNICATION CIRCUITS

L	T	P	C
3	0	0	3

This course aims to provide an understanding of signal degradation through broadband links, techniques to combat them, and integrated circuit implementation of these techniques. The term "broadband" refers to the class of signals which have significant spectral energy from very low frequencies to the data rate of the signal. i.e. signals that are not modulated on a carrier whose frequency far exceeds the bandwidth.

Course Objectives:

- To gain the designing knowledge of broadband communication circuits.
- To explain the concept of CMOS and current driven logic circuits.
- To understand the channel characteristics and designing issues.
- To design the circuits to reduce the effect of inter symbol interference.
- To learn the significance and realization of equalizers in broadband communication circuits.
- To design the transmit equalizers using flip-flops and transconductors.
- To understand the design of receiver equalizers. To impart the knowledge about clock and data recovery circuits.

Unit I **6L**

Introduction: Introduction to broadband digital communication, serializers and deserializers, power and delay in CMOS and current driven logic circuits, CMOS logic, single ended data transmission, limitations, current mode logic-basic circuit design, current mode logic-MUX, XOR, latch, current mode logic-latch design, current mode logic-latch characteristics.

Learning Outcomes:

After completion of this unit the student will be able to

- learn the overview of broadband digital communication Circuits (L1).
- understand the CMOS logic (L2).
- identify the limitations of single ended data transmission (L1).
- understand current mode logic for the design of MUX, XOR, latch (L2).

Unit II **8L**

Low pass transmission channel-Intersymbol interference, error rate, first order channel model, ISI, Jitter, eye opening, channel characteristics-intersymbol interference, crosstalk, equalizer design, equalizer design-minimizing the residual error, equalization-effect on noise and crosstalk, tradeoffs between equalization at Tx and Rx; design of Tx equalizers.

Learning Outcomes:

After completion of this unit the student will be able to

- understand the Transmission Channel Characteristics(L2).
- learn the concept of Inter symbol interference (L2).
- understand the Requirement of equalization (L3).
- explain the Effects of equalization on noise and crosstalk (L4).

Unit III **8L**

Design of Transmit Equalizers: Design of transmit equalizers using flip-flops and transconductors, Tx equalizer-design considerations; realizing variable coefficients, differential pair-effect of tail node capacitance, continuous time equalization, continuous-time equalizer realization, replica biasing for the tail current source, replica biasing, optimizing transmitter swing, replica biasing, optimizing transmitter swing, analog layout optimization.

Learning Outcomes:

After completion of this unit the student will be able to

- learn about the Transmit Equalizers (L2).
- identify the design considerations of an Equalizer (L5).
- understand continuous time equalization (L2).
- realize the continuous-time equalizer (L5).
- optimize the Transmitter swing (L1).
- understand analog layout optimization (L1).

Unit IV **8L**

Design of Receiver Equalizers: Equalization at the receiver; basics of adaptation, LMS adaptation, sign-sign LMS adaptation, LMS implementation details, adaptive equalizer implementation, S/H based equalizer, obtaining the gradients, multiplexed and demultiplexed PRBS sequences, latch vs. amplifier, zeros for pre- and post- cursor equalization, echo cancellation, decision feedback equalizers-elimination of noise enhancement, error propagation, BER analysis, implementation issues.

Learning Outcomes:

After completion of this unit the student will be able to

- learn about the concept of adaptation (L2).
- know the Different adaptation techniques (L3).
- learn the adaptive equalizer implementation (L4).
- understand S/H based equalizer (L2).
- to learn the Decision feedback equalizers (L3).

Unit V **8L**

Clock and Data Recovery: Frequency multiplication using a phase locked loop, Type I PLL; derivation of the phase model of the PLL, Tri state phase detector, reference feedthrough, tradeoff between reference feedthrough and lock range, stability of feedback loops; derivation of the type II PLL, realization of type II PLLs-charge pump, loop filter, reference feedthrough in a type II PLL; phase detector for random data, linear phase detector for random data, transfer functions in a PLL, binary phase detectors; bang bang jitter, optimal equalizers, linearity assumption of PLL model, PLL capture phenomenon, Hogge phase detector offset correction.

Learning Outcomes:

After completion of this unit the student will be able to

- learn the Basic operation of PLL (L1).
- understand the difference between type-I and type-II PLL (L2).
- realize the type-I PLL (L4).
- understand the concepts lock range, stability in Type-I PLL (L1).

- realize the type-II PLL (L4).
- learn Binary Phase Detectors (L1).
- understand the basic Hogge phase detector offset correction (L3).

Text Books

1. Behzad Razavi, Monolithic Phase Locked Loops and Clock Recovery Circuits-Theory and Design, IEEE Press, 1996,
2. Behzad Razavi, Phase Locking in High Performance Systems-From Devices to Architectures, IEEE Press, 2003,
3. Behzad Razavi, Design of Integrated Circuits for Optical Communications, McGraw-Hill, 2002,

References

1. William J, Dally, John W, Poulton, Digital Systems Engineering, Cambridge University Press, 1998,
2. IEEE Journal of Solid State Circuits, IEEE, http://ieeexplore,ieee,org

Course Outcomes:

After successful completion of the course, the student will be able to

- learn the overview of broadband digital communication Circuits (L1).
- understand current mode logic for the design of MUX, XOR, latch (L2).
- understand the Requirement of equalization (L3). □ realize the continuous-time equalizer (L5).
- learn the adaptive equalizer implementation (L4).
- realize the type-II PLL (L4).

19EEC770: LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

This course introduces the student, to Low Power in CMOS VLSI Circuit Design. The first unit covers the physics of power dissipation in MOSFET devices and circuits. The second unit describes power estimation and design & test of low-voltage CMOS circuits. The third unit explains low-energy computing using energy recovery techniques. The fourth unit gives details for Minimizing Energy Consumption and sub-threshold digital logic. The last unit describes the design of sub-threshold memory design.

Course Objectives:

- To familiarize the physics and various types of Power Dissipation in CMOS.
- To explain Power Estimation in CMOS.
- To impart the knowledge of Design and Test of Low Voltage CMOS Circuits.
- To introduce Low Energy Computing using Energy Recovery Techniques.
- To describe Inverter and SRAM in subthreshold.

Unit I **8L**

Physics of Power Dissipation in CMOS FET Devices: Physics of power dissipation in MOSFET devices, power dissipation in CMOS, low power VLSI design limits.

Learning Outcomes:

After completion of this unit the student will be able to

- identify the physics of power dissipation in MOSFET devices (L1).
- determine power dissipation on CMOS (L1).
- predict low-power VLSI design Limitation at different abstraction level (L1).

Unit II **8L**

Power Estimation: Modeling of signals, signal probability calculation, probabilistic techniques for signal activity estimation, statistical techniques, estimation of glitching power, sensitivity analysis. **Design and Test of Low Voltage CMOS Circuits**: Circuit design style, leakage current in deep sub micrometer transistors, deep submicrometer device design issues, key to minimizing SCE, low voltage circuit design techniques.

Learning Outcomes:

After completion of this unit the student will be able to

- state signal probability and activity (L2).
- identify statistical techniques for estimating average power (L2).
- predict power sensitivity using sensitivity analysis (L2).
- determine the glitching power and delay models (L2).

Unit III **8L**

Low Energy Computing using Energy Recovery Techniques: Energy dissipation in transistor channel using an RC model, energy recovery circuit design, designs with partially reversible logic

Learning Outcomes:

After completion of this unit the student will be able to

- state energy dissipation using an RC model (L4).
- identify the energy recovery circuits (L4).
- determine design with partially reversible logic (L4).

Unit IV **8L**

Minimizing energy consumption: Modelling minimum energy consumption, minimum energy point dependencies. **Digital Logic**: Inverter operation in Sub threshold, Sub threshold CMOS logic cell library.

Learning Outcomes:

After completion of this unit the student will be able to

- state sub-threshold leakage current models (L5).
- identify the other components of current (L5).
- determine the minimum energy point dependencies (L5). apply sub threshold operation on inverter (L5).

Unit V **8L**

Sub threshold Static RAM: SRAM over view, 6 Transistor SRAM bit cell in sub threshold, write operation, read operation, Static noise margin in sub threshold, A sub threshold bit cell design, reducing voltage swings on bit lines, reducing power in write driver circuits, reducing power in sense amplifier circuits.

Learning Outcomes:

After completion of this unit the student will be able to

- state static noise margin in sub threshold (L5).
- identify the write and read operation of 6T SRAM (L5).
- determine a sub-threshold bit-cell design (L5).

Text Books

1. Kaushik Roy &Sharat C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley and Sons, 2012. 2. Jan Rabaey, Low Power Design Essentials, Springer Publications, 2011.
2. Lice Wang,Benton Highsmith Calhoun, Anantha P Chandrakasan, Sub Threshold Design for Ultra- Low Power Systems, Springer Publications,2005

Course Outcomes:

After successful completion of the course, the student will be able to

- describe the physics of power dissipation in MOSFET (L1).
- list and describe various leakage power in CMOS (L2).
- identify low energy computing using energy recovery techniques (L4).
- analyze and design minimum energy consumption circuits (L4).
- explain the principles and operation of Inverter and SRAM in sub threshold (L5).

19EEC772: VLSI CAD

L	T	P	C
3	0	0	3

This course introduces to the student, to learn the concepts of VLSI Physical design to work in the VLSI Core industry. This course provides all the algorithms at each stage in the Physical design. First chapter discuss the terminology, second chapter explains the modelling and simulation processes and chapter 3 tells the concepts of logic verification and high level synthesis. The remaining chapters explain all the Physical design concepts.

Course objectives:

- To remember the graph terminology and data structures
- To explain Different graph algorithms and analyzing VLSI CAD problems categories
- To understand both gate level and switch level modelling procedure
- To understand and analyzes high level synthesis procedure and logic verification algorithms
- To explain layout compaction and partitioning algorithms
- To understand floor planning concepts and algorithms
- To understand routing procedures and techniques
- Finally, application of all the above concepts in the VLSI Physical Design field.

Unit I **6L**

Algorithmic Graph Theory and Computational Complexity – Terminology, data structures for the representation of graphs, computational complexity, examples of graph algorithms, depth-first search, breadth-first search, dijkstra's shortest-path algorithm, prim's algorithm for minimum spanning trees.

Learning outcomes:

After completion of this unit the student will be able to

- understands the representation, terminology and complexity in computation of graphs (L2).
- learns different graph algorithms (L1).
- applies search algorithms and compares them (L3).
- evaluating differences between different search algorithms (L5).
- understands tractable and intractable problems and apply for VLSI CAD problems (L4).

Unit II **6L**

Simulation: Gate-level modeling and simulation, signal modeling, gate modeling, delay modeling, connectivity modeling, compiler-driven simulation event-driven simulation, switchlevel modeling and simulation, connectivity and signal modeling.

Learning outcomes:

After completion of this unit the student will be able to

- understand the modelling and simulation procedures at gate and switch level (L2).
- apply delay modelling concept in gate level modeling (L3).
- understand static and dynamic partition concepts (L2).
- examine about simulation mechanism parts (L4).

Unit III **10L**

Logic Synthesis and Verification: Introduction to combinational logic synthesis, basic issues and terminology, a practical example, binary decision diagrams, ROBDD principles, ROBDD implementation and construction, ROBDD manipulation. **High-level Synthesis**: Hardware models for high-level synthesis, hardware for computations, data storage, and interconnection, data, control, and clocks, internal representation of the input algorithm.

Learning outcomes:

After completion of this unit the student will be able to

- understands the concept and terminology of logic synthesis and verification (L2).
- apply ROBBD concept on logic expression implementation (L3).
- understands hardware models for high level synthesis (L2).
- understand scheduling and sequencing algorithms (L2).

Unit IV **8L**

Layout Compaction: Design rules, symbolic layout, problem formulation, algorithms for constraint-graph compaction, a longest-path algorithm for dags, the longest path in graphs with cycles, the liao- wong algorithm, the bellman-ford algorithm, **Placement and Partitioning**: Circuit representation, wire-length estimation, types of placement problem, placement algorithms, constructive placement, iterative improvement, partitioning, the Kernighan-Lin partitioning algorithm.

Learning outcomes:

After completion of this unit the student will be able to

- understand the concepts of layout compaction, placement and partition (L2).
- analyze Liao-Wang and Bellman-Ford layout compaction algorithm (L4).
- understands constructive and iterative partitioning techniques (L2).
- analyze KL partitioning algorithm (L4).

Unit V **10L**

Floor planning: Floor planning concepts, terminology and floorplan representation, optimization problems in floor planning, shape functions and floorplan sizing. **Routing**: Types of local routing problems, area routing, channel routing, channel routing models, the vertical constraint graph, horizontal constraints and the left-edge algorithm channel routing algorithms.

Learning outcomes:

After completion of this unit the student will be able to

- understand the concepts of floor planning and routing (L2).
- apply floor planning optimizing techniques in shape function finding (L3).
- understand Global routing and constraints (L2).
- apply the concepts of Left edge algorithm in VLSI CAD applications (L3).

Text Books

1. S. H. Gerez, Algorithms for VLSI Design Automation, WILEY Student Edition, India, 2013.

References

1. Majid Sarrafzadeh and C, K, Wong, An Introduction to VLSI Physical Design, McGraw Hill, 2011.
2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, 3/e, Kluwer Academic, 2012.

3. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer Publications, 2011.

Course Outcomes:

After successful completion of the course, the student will be able to

- know the graph algorithms; identify tractable and intractable problems in VLSI CAD (L1)
- use the suitable simulator to reduce the time and space complexities (L2)
- explain the physical design process flow in the field of VLSI (L4)
- apply knowledge in VLSI industry as the Physical design engineer (L5)
- construct high level synthesis problems in finding the solutions (L3)

19EEC774: DIGITAL SYSTEMS TESTING AND TESTABILITY

L T P C
3 0 0 3

This course introduces the students, to testing and verification in VLSI design process. The first unit covers various fault models and their simulation. The next three units cover various ATPG methods to detect faults in combinational and sequential circuits. The last covers BIST schemes.

Course Objectives:

- To provide detection techniques for faults occurring in digital systems
- To explore glossary of fault models to simplifying the detection
- To generate test vectors to detect and diagnose the faults using various algorithms
- To provide knowledge about designing of Testable Combinational and Sequential circuits/Memory systems
- To recognize the BIST techniques for improving testability

Unit I **8L**

Introduction: VLSI Testing Process, Fault Modeling: Defects, errors and functional versus structural testing, levels of fault models, glossary of fault models, single stuck-at fault. Logic and Fault Simulation: Simulation for design verification, simulation for test evaluation, modeling circuits for simulation, algorithms for true-value simulation, algorithms for fault simulation, statistical methods for fault simulation.

Learning Outcomes:

After completion of this unit the student will be able to

- apply the concepts in testing which can help design a better yield in IC design (L1).
- use the appropriate test algorithm methods for achieving certain fault coverage specifications in design (L2).
- differentiate between defect, fault and error (L1).

Unit II **8L**

Combinational Circuit Test Generation: Algorithms and representations, redundancy identification (RID), testing as a global problem, definitions, significant combinational ATPG algorithms.

Learning Outcomes:

After completion of this unit the student will be able to

- identify the various test generation methods for combinational circuits (L2).
- apply ATPG methods to discover faults at functional level (L3).
- measure controllability and observability for testability (L3).

Unit III **8L**

Sequential Circuit Test Generation: ATPG for single-clock synchronous circuits, time-frame expansion method, simulation-based sequential circuit ATPG.

Learning Outcomes:

After completion of this unit the student will be able to

- extend combinational ATPG algorithms for test generation (L2).
- implement ATPG for cyclic and cycle-free circuits (L3).

Unit IV **8L**

Memory Test: Memory density and defect trends, faults, memory test levels, march test notation, fault modeling, memory testing Digital DFT and Scan Design: Ad-Hoc DFT methods, scan design, partial-scan design, variations of scan.

Learning Outcomes:

After completion of this unit the student will be able to

- separate memory fault types at different test levels (L1).
- build fault models for memory test (L2).
- distinguish various Scan methods for test generation and application in DFT (L3).

Unit V **8L**

Built-In Self-Test: The economic case for BIST, random logic BIST, memory BIST, delay fault BIST. Boundary Scan Standard: Motivation, system configuration with boundary scan, boundary scan description language.

Learning Outcomes:

After completion of this unit the student will be able to

- discuss BIST architecture (L1).
- classify different BIST Techniques used for Test Generation (L1).
- explain operation of elementary boundary scan cell (L2).
- identify boundary scan descriptive language for implementing boundary scan in any device (L3).

Text Books

1. M. Abramovici, M. A. Breuer, A. D. Friedman, Digital Systems Testing and Testable Design, Piscataway, IEEE Press, 2011.
2. M. L. Bushnel, V. D. Agarwal, Essentials of Testing for Digital, Memory and MixedSignal VLSI Circuits, Kluwer Academic Publishers, 2012.

References

1. 1.VLSI Test Principles and Architectures: Design For Testability by Laung-Terng Wang, cheng-Wen Wu, Xiaoqing Wen Kaufmann Morgan Publishers, 2006.
2. NirajJha, Sandeep Gupta, Test of Digital Systems, Cambridge University Press, 2010.
3. Robert J. Feugate, Steven M. McIntyre, Introduction to VLSI Testing, Prentice Hall Publications, 2010.

Course Outcomes:

Successful completion of the course, the student will be able to

- acquire knowledge about fault modeling and collapsing (L1).
- learn about various combinational ATPG (L2).
- understand sequential test pattern generation (L2).
- use various techniques such as BIST and Boundary scan (L3).

19EEC776: DATA CONVERTERS

L	T	P	C
3	0	0	3

This course introduces the student, working principles of Data converters and their architectures. The first unit introduces high-speed comparators and front-end circuits of data converters such as sample and hold circuits, and their circuit realizations. The second unit introduces ContinuousTime Filters and discrete-time signals and systems. The third unit introduces Switched-Capacitor circuits and fundamentals of data converters. The last two units introduce Nyquist-Rate Data converters and Oversampled converters.

Course Objectives:

- To introduce Op-Amp comparators, and circuit realizations and to analyze their performance.
- To familiarize Sample-And-Hold circuits, and their realizations, like CMOS, BiCMOS and Bipolar realizations.
- To explain Continuous-Time Filters and to introduce filter design based on OTA and using fixed resistors.
- To introduce Switched-Capacitor Circuits, and to analyze and derive transfer functions of higher order filters, and to explore issues like charge injection.
- To explain fundamentals of Data converters and to analyze their performance specifications.
- To introduce Sampling theorem and illustrate its application in the design of sampled rate data converters.
- To explain about the importance of oversampling and to illustrate oversampling in the design of data converters.

Unit I **8L**

Comparators: Comparator specifications, using an opamp for a comparator, charge-injection errors, latched comparators, examples of CMOS and BiCMOS comparators. **Sample-And-Hold and Translinear Circuits:** Performance of sample-and-hold circuits, MOS sample-and-hold basics, examples of CMOS s/h circuits, bipolar and BICMOS sample and holds, translinear gain cell, translinear multiplier.

Learning Outcomes:

After completion of this unit, the student will be able to design and analyze Op-Amp Comparators (L1).

- analyze latched comparators and to explore their design space (L2).
- analyze CMOS and BiCMOS comparators (L3).
- analyze the performance of Sample-and-hold circuits (L1).
- analyze CMOS and BiCMOS realization of Sample-and-hold circuits (L2).
- analyze Bipolar circuit realization of Sample-and-hold circuit (L2).
- analyze Translinear multiplier (L3).

Unit II **10L**

Continuous-Time Filters: Introduction to continuous-time filters, introduction to gm-c filters, transconductors using fixed resistors, CMOS transconductors using active transistors, BiCMOS transconductors, active RC and MOSFET-C filters, **Discrete-Time Signals:** Overview of some signal spectra, Laplace transforms of discrete-time signals, spectra of discrete-time signals, ztransform, down sampling and up sampling, discrete-time filters, Sample-and-hold response.

Learning Outcomes:

After completion of this unit, the student will be able to

- explain continuous-time filters (L1).
- design and analyze g_m-C filters and transconductors using fixed resistors (L2).
- design and analyze CMOS transconductors using active transistors (L3).
- design and analyze BiCMOS transconductors (L3).
- explore the design space of various filters for the given specifications (L4).
- explain discrete-time signals and systems and transforms (L1).
- analyze Frequency spectrum of discrete time signals (L2).

Unit III **8L**

Switched-Capacitor Circuits: Basic building blocks, basic operation and analysis, noise in switched-capacitor circuits, first-order filters, Biquad filters, charge injection, switched-capacitor gain circuits, **Data Converter Fundamentals**: Ideal D/A converter, ideal A/D converter, quantization noise, deterministic approach, stochastic approach, signed codes, performance limitations, resolution, offset and gain error, accuracy and linearity.

Learning Outcomes:

After completion of this unit, the student will be able to

- design and analyze Switched-Capacitor circuits and filters (L1).
- design and analyze Biquadratic transfer functions and filters (L2).
- understand and explain charge injection mechanism and identifying remedies (L3).
- identify and understand ideal DAC and ADC specifications (L1).
- understand the role of quantization in assessment of SNR of Data converters (L2).
- explore deterministic and stochastic approaches for the analysis of Data converters (L3).

Unit IV **8L**

Nyquist-Rate D/A Converters: Decoder-based converters, binary-scaled converters, thermometer-code converters, hybrid converters, **Nyquist-rate A/D converters:** integrating converters, successive-approximation converters, pipelined A/D converters, flash converters, issues in designing flash A/D converters, two-step A/D converters.

Learning Outcomes:

After completion of this unit, the student will be able to

- explain various types of Decoder based DACs and also analyze their performance (L1).
- design and analyze Binary scaled converters (L2).
- design and analyze thermometer-code converters (L2).
- understand the working principle of hybrid converters and design for the given specifications (L4).
- design and analyze integrating type ADCs (L2).
- design and analyze Successive-Approximation type ADCs (L2).
- design and analyze pipelined ADCs (L3).
- design and analyze Flash type ADCs (L3).
- design and analyze two-step ADCs (L4).

Unit V **8L**

Oversampling Converters: Oversampling without noise shaping, oversampling with noise shaping, system architectures, digital decimation filters, higher-order modulators, bandpass oversampling converters, practical considerations.

Learning Outcomes:

After completion of this unit, the student will be able to

- explain oversampled systems (L1).
- explain noise shaping (L2).
- explain oversampled data converters with noise shaping (L3).
- design and analyze System architectures for Oversampled data converters (L4).
- design and analyze System architectures for higher order modulators (L5).

Text Books

1. Tony Chan Carusone, Kenneth W, Martin, David A, Johns, Analog Integrated Circuit Design, 2nd Edition, Wiley Publications 2011,
2. Allen Holberg, CMOS Analog Circuit Design, 2/e, Oxford Publications, 2012

References

1. CMOS Data Converters for Communication - M, Gustavsson, J, Wikner, and N, Tan, Kluwer Academic Publishers, 2009.
2. Behzad Razavi, Principles of Data Conversion System Design, IEEE Press, 2010.
3. CMOS Mixed Signal Design, Baker Li, Boyce, Wiley Publications, 2011.

Course Outcomes:

After successful completion of the course, the student will be able to

- design and analyze Nyquist rate sampled and over sampled Data converters (L4).
- design and analyze High speed comparators (L3).
- design and analyze Switched capacitor circuits (L2).
- design and analyze Continuous-time and Discrete-time filters (L2). □ design and analyze Sample and hold systems (L1).

19EEC778 - CIRCUITS FOR ANALOG SYSTEM DESIGN

L T P C
3 0 0 3

Module I **8 Hours**

Transistor as a switch, transistor as amplifier, problems in the transistor amplifier, temperature drift and device to device variation, 3-transistor op amp, use of op-amp for different applications and basic issues in use of op amps, designing a linear power supply using op amp, selection of components.

Module II **8Hours**

Design of heat sink and design of transformer for the linear power supply, design of low drop out regulators, design of temperature indicator using IC sensors, errors due to resistance drift, opamp offset voltage drift, offset current drift, error budgeting, design of an on/off temperature controller, design of different types of heater drive circuits, thyristor and transistor based drive circuit design, error budgeting.

Module III **8 Hours**

Design of proportional temperature controller circuit using thermocouple temperature sensor, error budgeting, design of heater drive circuits using triacs and transistors, use of pulse width modulation circuits, use of MOSFETs and IGBTs, short circuit protection techniques.

Module IV **8 Hours**

Design of PID temperature controllers, basics of PID parameter selection, design of constant current sources with error budgeting, design of 4-20ma current transmitter for resistance sensors, design of 4-20ma current transmitter for LVDT sensor, design of oscillator circuits, errors in the op amp circuit for ac amplifiers, errors in ac application.

Module V **8 Hours**

Use of instrumentation amplifier and its basis, designing of a capacitor measurement circuit, ratio transformer technique, differential capacitor measurement, errors in the capacitance measurement, phase sensitive detection and use of the same for lock-in amplifier design, ADC/DAC converter types, use of ratio metric converters, error budgeting for the different types of ADC/DAC, band gap zenors and other reference diodes.

Text / References

1. Franco S, Design with Operational Amplifiers and Analog Integrated Circuits, McGraw Hill, 2010.
2. Paul Horowitz & Winfield Hill, The Art of Electronics, 2/e, Cambridge University Press, 2011.

19EEC779 - COMPUTER ARITHMETIC

L T P C
3 0 0 3

Module I **8 Hours**

Number Representation: Numbers and arithmetic,what is computer arithmetic?, motivating examples, numbers and their encodings, fixed-radix positional number systems, number radix conversion, classes of number representations. **Representing signed numbers:** signed-magnitude representation, biased representations, complement representations, two's and 1's-complement numbers, direct and indirect signed arithmetic, using signed positions or signed digits. **Redundant number systems**: coping with the carry problem, redundancy in computer arithmetic, digit sets and digit-set conversions, generalized signed-digit numbers.

Module II **8 Hours**

Addition/Subtraction: Basic addition and counting, bit-serial and ripple-carry adders, conditions and exceptions, analysis of carry propagation, carry completion detection, addition of a constant, counters, manchester carry chains and adders. **Carry-lookahead adders**: unrolling the carry recurrence, carry-lookahead adder design, ling adder and related designs, carry determination as prefix computation, alternative parallel prefix networks, VLSI implementation aspects.

Module III **8 Hours**

Multiplication: Shift/add multiplication algorithms, programmed multiplication, basic hardware multipliers, multiplication of signed numbers, multiplication by constants, preview of fast multipliers. **High-radix multipliers**: radix-4 multiplication, modified booth's recoding, using carry-save adders.

Module IV **8 Hours**

Division: Basic Division Schemes: Shift/subtract division algorithms, programmed division, restoring hardware dividers, non-restoring and signed division, division by constants, radix-2 SRT division. **High-radix dividers:** Basics of high-radix division, using carry-save adders, radix-4 SRT division,

Module V **8 Hours**

Real Arithmetic: Floating-point representations, the ANSI/IEEE floating-point standard, basic floating-point algorithms, conversions and exceptions, rounding schemes, logarithmic number systems. **Floating-Point Operations**: Floating-point adders/subtractors, pre- and postshifting, rounding and exceptions, floating-point multipliers and dividers

Text Book

1. B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2/e, Oxford University Press, New York, 2010.

References

1. Israel Koren, Computer Arithmetic Algorithms, 2/e, Prentice Hall Publications, 2011.
2. Milos D.Ercegovac, Digital Arithmetic, The Morgan Kaufmann Series, 2012.

19EEC780 - COMPUTER ARCHITECTURE

L T P C
3 0 0 3

Module I **8 Hours**

Fundamentals of Computer Design: Technology trends, cost Measuring and reporting, performance quantitative principles of computer design. **Instruction set principles and examples**: Classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set, instruction for control, encoding an instruction set.

Module II **8 Hours**

Pipelining: Introduction, the major hurdle of pipelining-pipeline hazards, how is pipelining implemented?, what makes pipelining hard to implement?, extending the MIPS pipeline to handle multicycle operations. **Instruction Level Parallelism**: Overcoming hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP, ILP software approach, compiler techniques, static branch protection VLIW approach.

Module III **8 Hours**

Memory Hierarchy Design: Introduction, review of the abcs of caches, cache performance, reducing cache miss penalty, reducing miss rate, reducing cache miss penalty or miss rate via parallelism, reducing hit time, main memory and organizations for improving performance, memory technology, virtual memory, protection and examples of virtual memory, basics of virtual machines.

Module IV **8 Hours**

Multiprocessors and Thread-Level Parallelism: Introduction, characteristics of application domains, symmetric shared-memory architectures, performance of symmetric shared-memory multiprocessors, distributed shared-memory architectures, performance of distributed shared-memory multiprocessors, synchronization. **Models of memory consistency**: an introduction, multithreading, exploiting thread-level parallelism within a processor.

Module V **8 Hours**

Storage Systems: Introduction, types of storage devices, buses-connecting I/O devices to cpu/memory, reliability, availability, and dependability, raid, redundant arrays of inexpensive disks, errors and failures in real systems, I/O performance measures, designing an I/O system in five easy pieces.

Text Book

1. John L, Hennessy & David A Patterson, Computer Architecture a quantitative approach, 3/e, Morgan Kuffman, 2011.

References

1. John L, Hennessy & David A Patterson, Computer Architecture a quantitative approach, 4/e, Morgan Kuffman, 2012.
2. Kai Hwang and A. Briggs, Computer Architecture and Parallel Processing, International Edition, McGraw Hill, 2011.
3. DezsoSima, Terence Fountain, Peter Kacsuk, Advanced Computer Architecture, Pearson Education, 2011.

19EEC781 - ARM SYSTEM DEVELOPMENT

L T P C
3 0 0 3

Module – I **8 Hours**

ARM Introduction and Pipeline structures: Types of computer Architectures, ISA's and ARM History. Embedded System Software and Hardware, stack implementation in ARM, Endianness, condition codes. Processor core VS CPU core, ARM7TDMI Interface signals, Memory Interface, Bus Cycle types, Register set, Operational Modes. Instruction Format, ARM Core Data Flow Model, ARM 3 stage Pipeline, ARM family attribute comparison. ARM 5 stage Pipeline, Pipeline Hazards, Data forwarding - a hardware solution.

Module – II **8 Hours**

ARM7TDMI assembly instructions and modes: ARM ISA and Processor Variants, Different Types of Instructions, ARM Instruction set, data processing instructions. Shift Operations, shift Operations using RS lower byte, Immediate value encoding. Dataprocessing Instructions.AddressingMode-1, Addressing Mode -2. Addressing Mode -2, LDR/STR, Addressing mode -3 with examples. Instruction Timing, Addressing Mode - 4 with Examples. Swap Instructions, Swap Register related Instructions, Loading Constants. Program Control Flow, Control Flow Instructions, B & BL instructions, BX instruction.Interrupts and Exceptions, Exception Handlers, Reset Handling.Aborts, software Interrupt Instruction, undefined instruction exception. Interrupt Latency, Multiply Instructions, Instruction set examples. Thumb state, Thumb Programmers model, Thumb Implementation, Thumb Applications. Thumb Instructions, Interrupt processing. Interrupt Handelling schemes, Examples of Interrupt Handlers.

Module – III **8 Hours**

ARM Coprocessor Interface and VFP: ARM coprocessor interface and Instructions, Coprocessor Instructions, data Processign Instruction, data transfers, register transfers. Number representations, floating point representation (IEEE754). Flynn's Taxonomy, SIMD and Vector Processors, Vector Floating Point Processor (VFP), VFP and ARM interactions, An example vector operation.

Module – IV **8 Hours**

Cache and Memory Management and Protection: Memory Technologies, Need for memory Hierarchy, Hierarchical Memory Organization, Virtual Memory. Cache Memory, Mapping Functions. Cache Design, Unified or split cache, multiple level of caches, ARM cache features, coprocessor 15 for system control. Processes, Memory Map, Protected Systems, ARM systems with MPU, memory Protection Unit (MPU). Physical Vs Virtual Memory, Paging, Segmentation. MMU Advantage, virtual memory translation, Multitasking with MMU, MMU organization, Tightly coupled Memory (TCM).

Module – V **8 Hours**

ARM tools and Peripherals: ARM Development Environment, Arm Procedure Call Standard (APCS), Example C program. Embedded software Development, Image structure, linker inputs and outputs, memory map, application startup. AMBA Overview, Typical AMAB Based Microcontroller, AHB bus features, AHB Bus transfers, APB bus transfers, APB bridge. DMA, Peripherals, Programming Peripherals in ARM. ARM ISAs, ARMv5, ARMv6, ARM v7, big.little technology, ARMv8. ARM ISAs, ARMv5, ARMv6, ARM v7, big.little technology, ARMv8.

References

1. ARM System Developers Guide, Designing and Optimizing System Software, by Andrew N. SLOSS, Dominic SYMES and Chris WRIGHT, ELSEVIER, 3004
2. ARM System-on-Chip Architecture, Second Edition, by Steve Furber, PEARSON, 2013
3. Operating Systems, 5th Edition, By William Stallings
4. Manuals and Technical Documents from the ARM Inc, web site.

19EEC782 - ADVANCED COMPUTER ORGANIZATION

L T P C
3 0 0 3

Module I **8 Hours**

Instruction Set Architecture: Memory locations and addresses, memory operations, instructions and instruction sequencing, addressing modes, assembly language, stacks, subroutines, additional instructions, dealing with 32-bit immediate values, CISC instruction sets, RISC and CISC styles, example programs, encoding of machine instructions.

Module II **8 Hours**

Basic Input/Output: Accessing I/O Devices, interrupts**. Software:** The assembly process, loading and executing object programs, linker, libraries, compiler, debugger, high level language for I/O tasks, interaction between assembly and c language, the operating system.

Module III **8 Hours**

Basic Processing Unit: Some fundamental concepts, instruction execution, hardware components, instruction fetch and execution steps, control signals, hardwired control, CISC-style processors. **Pipelining:** Basic concept—the ideal case, pipeline organization, pipelining issues, data dependencies, memory delays, branch delays, resource limitations, performance evaluation

Module IV **8 Hours**

Input/Output Organization: Bus structure, bus operation, arbitration, interface circuits, interconnection standards. **The Memory System:** Basic concepts, semiconductor ram memories, read-only memories, direct memory access, memory hierarchy, cache memories, performance considerations, virtual memory, memory management requirements, secondary storage.

Module V **8 Hours**

Arithmetic: Addition and subtraction of signed numbers, design of fast adders, multiplication of unsigned numbers, multiplication of signed numbers, fast multiplication, integer division, floating-point numbers and operations. **Parallel Processing and Performance**: Hardware multithreading, vector (SIMD) processing, shared-memory multiprocessors, cache coherence, message-passing multicomputers,

Text Books

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky & Naraig Manjikian, Computer Organization and Embedded Systems, 6/e, McGraw Hill Publications, 2010

Reference

1. Patterson, Hennessy, Computer Organization and Design, 4/e, Elsevier Publications, 2011.
2. Kai Hwang and A. Briggs, Computer Architecture and Parallel Processing, International Edition McGraw Hill, 2012.
3. DezsoSima, Terence Fountain, Peter Kacsuk, Advanced Computer Architecture, Pearson Education, 2011.

19EEC783 - OPERATION AND MODELING OF MOS TRANSISTOR

L T P C
3 0 0 3

Module I **8 Hours**

Semiconductors, Junctions, and MOSFET Overview: Introduction, semiconductors, conduction contact potentials, the PN-junction, overview of the MOS transistors, fabrication processes and device features. **The Two Terminal MOS Structure:** Introduction, the flat-band voltage, potential balance and charge balance, effect of gate - body voltage on surface condition, accumulation and depletion, inversion, small - signal capacitance, summary of properties of the regions of inversion

Module II **8 Hours**

The Three Terminal MOS Structure: Introduction, contacting the inversion layer, the body effect, regions of inversion, "CB control" point of view. **The Four - Terminal MOS Transistor**: Introduction, transistor regions of operation, complete all - region model, simplified all - region models, models based on quasi - Fermi potentials, regions of inversion in terms of terminal voltages, strong inversion, complete strong - inversion model, weak inversion special conditions in weak inversion , moderate inversion and single - piece models, source - referenced vs. body - referenced modeling, effective mobility, effect of extrinsic source and drain series resistances, temperature effects, breakdown, the p-channel MOS transistor

Module III **8 Hours**

Small Dimension Effects: Introduction, carrier velocity saturation, channel length modulation, charge sharing, drain - induced barrier lowering, punch through, combining several small - dimension effects into one model - a strong inversion example, hot carrier effects; impact ionization, velocity overshoot and ballistic operation, polysilicon depletion, quantum mechanical effects, dc gate current, junction leakage; band - to - band tunneling; GIDL, leakage currents – examples, the quest for ever - smaller devices.

Module IV **8 Hours**

The MOS Transistor In Dynamic Operation - Large Signal Modeling: Introduction, quasi - static operation, terminal currents in quasi - static operation, evaluation of intrinsic chargers in quasi - static operation, transit time under dc conditions, limitations of the quasi - static model, non - quasi - static modeling, extrinsic parasitics,

Module V **8 Hours**

Small - Signal Modeling for Low and Medium Frequencies: Introduction, a low - frequency small - signal model for the intrinsic part, a medium - frequency small - signal model for the intrinsic part, including the extrinsic part, all - region models. **High Frequency Small - Signals Models:** introduction, a complete quasi - static model, y- parameter models, non - quasi - static models.

Text Book

1. Yannis Tsividis and Colin McAndrew, Operation and Modeling of the MOS Transistor, 3/e, Oxford University Press, 2011.

References

1. Taur and Ning, Fundamentals of Modern VLSI Devices, 2/e, Cambridge University Press, 2012.
2. Donald Neamen, Semiconductors Physics and Devices, Tata Mc Graw Hill, 2012.
3. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley Publications, 2011.

19EEC784 - DIGITAL SYSTEMS ENGINEERING

L T P C
3 0 0 3

Module I **8 Hours**

Introduction: Engineering view of a digital system, technology trends and digital systems engineering, packaging of digital systems, a typical digital system, on chip wiring, integrated circuit packages, printed circuit boards, chassis and cabinets, backplanes and mother boards, wire and cable, connectors. **Modeling and Analysis of Wires:** Geometry and electrical properties, electrical models of wires, simple transmission lines, special transmission lines, wire cost models.

Module II **8 Hours**

Power Distribution: The Power supply network, local regulation, logic loads and on chip supply distribution, power supply isolation, bypass capacitors, example power distribution system. **Noise in Digital Systems:** Noise sources in a digital system, power supply noise, crosstalk, intersymbol interference, managing noise.

Module III **8 Hours**

Signaling Conventions: A Comparison of two transmission systems, considerations in a transmission system design, signaling modes for transmission lines, signaling over lumped transmission media, signal encoding. **Advanced Signaling Conventions:** Signaling over RC interconnect, driving lossy LC lines,

Module IV **8 Hours**

Timing Conventions: A comparison of two timing conventions, considerations in timing design, timing fundamentals, encoding timing, signals and events, open loop synchronous timing, closed loop timing, clock distribution. **Synchronization:** A comparison of two synchronization strategies, synchronization fundamentals, synchronizer design

Module V **8 Hours**

Signalling Circuits: Terminations, transmitter circuits, receiver circuits, ESD protection, an example signaling system. **Timing Circuits:** Delay line circuits, voltage controller oscillators, phase comparators, loop filters, clock aligners.

Text Books

1. William J. Dally and John Poulton, Digital Systems Engineering, Cambridge University Press, 2010

References

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, 3/e, McGraw Hill, 2012.
2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits, 3/e, McGraw Hill, 2012.
3. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2011.

19EEC785 - DSP ALGORITHMS AND IMPLEMENTATIONS

L T P C
3 0 0 3

Module I **8 Hours**

Review of Digital signal processing: The sampling process, discrete time sequences, discrete Fourier transform and FFT, linear time–invariant systems, digital filters, decimation and interpolation, analysis and design tool for DSP systems. **Computational accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.

Module II **8 Hours**

Architectures for Programmable DSP Devices: Basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing. **Programmable Digital Signal Processors:** Introduction, commercial digital signal processing devices, the architecture of TMS320c54xx digital signal processors, addressing modes of the TMS320c54xx processors, memory spaces of TMS320c54xx processors, program control, TMS320c54xx instructions and programming, on-chip peripherals. Interrupts, pipeline operation of the TMS320c54xx processors.

Module III **8 Hours**

Implementation of Basic DSP Algorithms: Introduction, the Q-notation, FIR filters, IIR filters, interpolation filters, decimation filters, PID controller, adaptive filters, 2-D signal processing. **Implementation of FFT Algorithms:** Introduction, an FFT algorithm for DFT computation, a butterfly computation, overflow and scaling, bit-reversed index generation, an 8-point FFT implementation of TMS320c54xx.

Module IV **8 Hours**

Interfacing Memory and Parallel IO Peripherals to Programmable DSP Devices: Introduction, memory space organization of the TMS320C54xx devices, memory and I/O signals of the TMS320C54xx devices, memory interface, parallel I/O, programmed I/O, interrupts and I/O, direct memory access (DMA).

Module V **8 Hours**

Interfacing Serial Converters to a Programmable DSP Device: Introduction, synchronous serial interface between the DSP and an AIC, a multi-channel buffered serial port (McBSP), the McBSP programming, a CODEC interface circuit, CODEC programming, a CODEC-DSP interface example.

Text Books

1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Cengage Learning, India, 2012.

References

1. Rulph Chassaing, Digital Signal Processing with C6713 and C6416 DSK, 2/e Wiley Publications, 2013.
2. DSP processor fundamentals, Architecture & Features-Lapsley et al. S. Chand & Co, 2012.
3. Steve Tretter, Communication System Design using DSP Algorithms, Springer Publications, 2011

19EEC786 - VLSI PHYSICAL DESIGN AUTOMATION

L T P C
3 0 0 3

Course Description:

This course emphasis the fundamentals algorithms used for VLSI Back End flow. Specifically this course emphasis the techniques for static timing analysis, partitioning, floorplanning, placement, routing and clock distribution

Course Educational Objectives:

1. To introduce the need of EDA tools for VLSI Physial Design Automation
2. To acquaint the students with timing constraints and analysis concepts
3. To expose the students to algorithms for partitioning and chip planning
4. To acquaint the students with placement and routing algorithms
5. To expose the students to design concerns during power routing and clock distribution

UNIT 1 Introduction to VLSI Physical Design 8 hours

Introduction to VLSI Physical Design, Introduction, Physical Design flow, Physical Verification, EDA Tools for Physical Design, Data Structures and Algorithms for Physical Design

Unit 2 Static Timing Analysis 8 Hours

Static Timing Analysis: Introduction (STA, DTA, Behaviour of synchronous circuit, Timing Arcs and Unateness, Definitions – Setup, Hold, Latch, Flipflop, STA (Flipflop) STA (Flipflop), STA (Latch), Time Borrowing and Time Stealing, Time Borrowing and Time Stealing – 2, OCV and CRPR, Multi-Mode Multi corner Analysis, Statistical Static Timing Analysis.

UNIT 3 Partitioning and Chip Planning 8 hours

Partitioning: Introduction and Optimization goals, KL – Algorithm, Extensions of KL – Algorithm, FM – Algorithm, Multilevel Partitioning, Chip Planning: Introduction and Optimization goals, Floorplanning Representations, Floorplanning Algorithms – 1, Floorplanning Algorithms, Pin Assignment.

UNIT 4 Placement and Routing Algorithms 8 hours

Placement. Introduction and Optimization goals, Min-cut placement, Analytic Placement, Simulated Annealing, Modern Placement Algorithms. Routing – Global and Detailed Introduction and optimization goals. Single net routing (Rectilinear routing) Global routing in the connectivity graph, Finding shortest paths with Dijkstra's Algorithm Horizontal and vertical constraint graphs Routing – Global and Detailed. Channel Routing Algorithms, Switch box routing algorithms, Over the cell routing algorithms

Unit 5: Special Routing: Power and Clock routing 8 Hours

Power and Ground routing, Unified Power Format and Special cells used for Power Planning, Clock Routing, Clocking Schemes and Design Considerations, Clock Routing algorithms – 1 (H-tree based and MMM algorithms), Clock Routing algorithms – 2 (Geometric matching and Weighted center algorithms), Clock Routing algorithms – 3 (Exact zero skew and DME algorithm), Skew, Latency, Uncertainty, and Jitter, Input Files for VLSI Physical Design flow, Input Files: Physical Library, Technology Library (LEF), Standard Cell Technology Library (LEF). Logical Library of Standard Cells: Operating Conditions, NLDM/ECSM models, Timing Desing Rule Constraints, Timing Desing Rule Constraints, Transition Table, Delay Table, Power Table, Parasitic Extraction, Wire Load Models, and RC table

Textbooks:

1. Prof. Bishnu Prasad Das, VLSI Physical Design and Timing Analysis, https://nptel.ac.in/courses/108107380
2. Sneh Saurabh, Introduction to VLSI Design Flow, Cambridge University Press, 2021.

References:

1. Sung Kyu Lim,Practical Problems in VLSI Physical Design, Springer,2008
2. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley ,1998
3. N.A.Sherwani , “Algorithms for VLSI Physical Design Automation”, (3/e),Kluwer,1999
4. M. Sait , H. Youssef, “VLSI Physical Design Automation”, World scientific, 1999
5. M.Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996
6. Habib Youssef, VLSI Physical Design Automation, World Scientific,2001

Course Outcomes:

By the end of the course, the student will be able to

1. Elaborate the need of EDA tools for VLSI Physical Design Automation
2. Analyse timing paths and fix them for setup and hold violations
3. Describe the algorithms for partitioning and chip planning
4. describe placement and routing algorithms with awareness of timing, area and power
5. elaborate and compare the different algorithms for power routing and clock distribution

19EEC787 - VLSI CAD

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Module I **10 Hours**

Algorithmic Graph Theory and Computational Complexity – Terminology, data structures for the representation of graphs, computational complexity, examples of graph algorithms, depth-first search, breadth-first search, dijkstra's shortest-path algorithm, prim's algorithm for minimum spanning trees. **Tractable and Intractable Problems**: Combinatorial optimization problems, decision problems, complexity classes, np-completeness and np-hardness.

Module II **10 Hours**

Simulation: Gate-level modeling and simulation, signal modeling, gate modeling, delay modeling, connectivity modeling, compiler-driven simulation event-driven simulation, switch-level modeling and simulation, connectivity and signal modeling.

Module III **10 Hours**

Logic Synthesis and Verification: Introduction to combinational logic synthesis, basic issues and terminology, a practical example, binary-decision diagrams, ROBDD principles, ROBDD implementation and construction, ROBDD manipulation, variable ordering. **High-level Synthesis:** Hardware models for high-level synthesis, hardware for computations, data storage, and interconnection, data, control, and clocks, internal representation of the input algorithm, allocation, assignment and scheduling, some scheduling algorithms

Module IV **10 Hours**

Layout Compaction: Design rules, symbolic layout, problem formulation, algorithms for constraint-graph compaction, a longest-path algorithm for dags, the longest path in graphs with cycles, the liao- wong algorithm, the bellman-ford algorithm, **Placement and Partitioning:** Circuit representation, wire-length estimation, types of placement problem, placement algorithms, constructive placement, iterative improvement, partitioning, the Kernighan-Lin partitioning algorithm.

Module V **10 Hours**

Floorplanning: Floorplanning concepts, terminology and floorplan representation, optimization problems in floorplanning, shape functions and floorplan sizing. **Routing:** Types of local routing problems, area routing, channel routing, channel routing models, the vertical constraint graph, horizontal constraints and the left-edge algorithm channel routing algorithms, introduction to global routing, standard-cell layout, building-block layout and channel ordering, algorithms for global routing

Text Books

1. S. H. Gerez, Algorithms for VLSI Design Automation, WILEY Student Edition, India, 2013.

References

1. Majid Sarrafzadeh and C, K, Wong, An Introduction to VLSI Physical Design, McGraw Hill, 2011.
2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, 3/e, Kluwer Academic, 2012.
3. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer Publications, 2011.

19EOE742: BUSINESS ANALYTICS

L T P C
3 0 0 3

This course introduces students to the science of business analytics. The goal is to provide students with the foundation needed to apply data analytics to real-world challenges they confront daily in their professional lives. Students will learn to identify the ideal analytic tool for their specific needs; understand valid and reliable ways to collect, analyze, and visualize data; and utilize data in decision making for managing agencies, organizations or clients in their workspace

Course Objectives:

- To familiarize the scope, process and advantages of business analytics
- To acquaint the student with the modeling and problem solving skills in business analytics
- To impart the organization and management of business analytics
- To introduce the forecasting models and techniques used in analytics
- To expose the formulation and decision strategies used in business analytics

Unit I **8L**

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the scope and process of business analytics (L1).
- choose an organizational structure to implement a business analytics process (L4).
- describe the statistical tools and methods used for data modeling and analysis (L2).
- identify the sampling and estimation requirements for data analysis (L1).

Unit II **8L**

Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

Learning Outcomes:

After the completion of this unit, the student will be able to

- identify the relationships and trends in data (L1).
- utilize linear regression methods for identifying data relationships (L4).
- list the types of data and their models used for business analytics (L1). describe the methods for visualization and exploration of data (L2).

Unit III **8L**

Organization Structures of Business analytics: Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the management issues in the organization structures (L2).
- define the designing information policy and its usage (L1).
- list the methods for ensuring data quality measuring contribution (L1).
- explain the use of data mining methodologies for predictive analytics analysis (L3).
- describe the use of prescriptive analytics methods in business analytics process (L2).

Unit IV **10L**

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Learning Outcomes:

After the completion of this unit, the student will be able to

- classify and describe the use of forecasting models (L3).
- model the use of regression forecasting with casual variables (L5).
- identify the appropriate forecasting model for a given data (L5).
- explain the use of monte carlo simulation for forecasting and identify the involved risk (L2).

Unit V **8L**

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Learning Outcomes:

After the completion of this unit, the student will be able to

- formulate decision problems (L2).
- list the decision strategies with and without probabilities (L1).
- use the decision trees for analysis (L4).
- describe the value of information, utility and its use in decision making (L4).

Textbook(s):

1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Business analytics Principles, Concepts, and Applications Pearson FT Press, 2014.
2. James Evans, Business Analytics, Pearson Education, 2013.

Course Outcomes:

Upon successful completion of the course, the student will be able to

- define the scope, process and advantages of business analytics (L1).
- explain the modeling and problem solving skills in business analytics (L2).
- describe the organization and management of business analytics (L3).
- utilize the forecasting models and techniques used in analytics (L4).
- enumerate and utilize the formulation and decision strategies (L2).

19EOE746: OPERATIONS RESEARCH

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Optimization problems arise in all walks of human activity- particularly in engineering, business, finance and economics. The simplest optimization problems are linear in nature which may be subject to a set of linear constraints. This course will equip the student with the expertise to mathematically model real life optimization problems as Linear Programming (Optimization) Problems and subsequently educate the student to solve these models with the help of the available methods.

Course Objectives:

- To impart knowledge on developing mathematical formulation for linear programming and transportation problem
- To familiarize the student in the construction of the required activities in an efficient manner to complete it on or before a specified time limit and at the minimum cost.
- To expose the development of mathematical model for interactive decision-making situations, where two or more competitors are involved under conditions of conflict and competition.
- To illustrate PERT and CPM techniques for planning and implementing projects.
- To impart the knowledge of formulating and analysis of real life problems using advanced tools and techniques for resource optimization
- To provide frameworks for analyzing waiting lines using advanced queuing theory concepts

Unit I **8L**

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Learning Outcomes:

After completing this unit, the student will be able to

- identify and develop operational research models from the verbal description of the real system (L4).
- understand the classification systems of effective Inventory control models (L2).

Unit II **8L**

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Learning Outcomes:

After completing this unit, the student will be able to

- translate a real-world problem, given in words, into a mathematical formulation (L2)
- utilize the mathematical tools that are needed to solve optimization problems (L2)

Unit III **8L**

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Learning Outcomes:

After completing this unit, the student will be able to

- describe the need and origin of the optimization methods (L2).
- classify optimization problems to suitably choose the method needed to solve the particular type of problem (L3).

Unit IV **8L**

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Learning Outcomes:

After completing this unit, the student will be able to

- choose linear programming problems to suitably choose the method needed to solve the particular type of problem (L1).
- identify industrial problems involved in inventory, MRP and scheduling (L2).

Unit V **8L**

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

Learning Outcomes:

After completing this unit, the student will be able to

- identify the values, objectives, attributes, decisions, uncertainties, consequences, and tradeoffs in a real decision problem (L2).
- apply the models to incorporate rational decision-making process in real life situations (L3).
- analyze various modeling alternatives & select appropriate modeling techniques for a given situation (L3).

Text Book(s):

1. H.A. Taha, Operations Research, An Introduction, Prentice Hall of India, 2008
2. H.M. Wagner, Principles of Operations Research, Prentice Hall of India, Delhi, 1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, 2008
4. Hitler Libermann Operations Research: McGraw Hill Publishers, 2009
5. Pannerselvam, Operations Research: Prentice Hall of India, 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India, 2010

Course Outcomes:

After the successful completion of the course, the students will be able to

- Understand the basic concepts of different advanced models of operations research and their applications (L2).
- Solve linear programming problems using appropriate techniques and optimization solvers, interpret the results obtained and translate solutions into directives for action (L4).
- Apply the models to incorporate rational decision-making process in real life situations (L4).

- Analyze various modeling alternatives & select appropriate modeling techniques for a given situation (L3).
- Validate output from model to check feasibility of implementations (L5).
- Create innovative modeling frameworks for a given situation (L6).
- Conduct and interpret post-optimal and sensitivity analysis and explain the primal-dual relationship (L3).

19EOE748: COST MANAGEMENT OF ENGINEERING PROJECTS

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This course will equip the student with the expertise to mathematically model engineering projects and use effective methods and techniques to plan and execute engineering activities.

Course Objectives:

- To introduce the basic principles of strategic cost management and the related terminology
- To familiarize the project planning and execution process involving technical/nontechnical activities
- To acquaint the student with detailed engineering activities and their cost management analysis
- To impart the knowledge of cost analysis and profit planning of engineering projects
- To familiarize the quantitative techniques for optimization of budget allocation

Unit I **8L**

Introduction and Overview of the Strategic Cost Management Process, Cost concepts in decisionmaking; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the cost concepts in decision making (L2).
- define the various costs involved in the cost management process (L2).
- list the objectives of cost control (L2).
- identify the different fields of a database for operational control (L2).

Unit II **8L**

Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the meaning of a project and list the different types (L2).
- identify the measures to manage cost overruns (L2).
- describe the various stages of project execution from conception to commissioning (L2).
- plan the proper order of technical/nontechnical activities as part of project execution (L2).

Unit III **8L**

Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

Learning Outcomes:
After the completion of this unit, the student will be able to
- identify the different clearance norms required in the pre-project execution phase (L2).
- describe the hierarchy of project team and identify the role of each member (L2).
- list the different contents of project contracts (L2).
- present the project cost control and planning through bar charts, network diagrams etc (L2).

Unit IV **8L**

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decisionmaking problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and ValueChain Analysis.

Learning Outcomes:
After the completion of this unit, the student will be able to
- describe the cost behavior and profit planning (L2).
- distinguish between marginal costing and absorption costing (L2).
- analyze the variance of standard costing (L2).
- analyze the pricing strategies in project costing (L2).
- identify the quality measures satisfying the appropriate constraints (L2).

Unit V **10L**

Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing. Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory

Learning Outcomes:
After the completion of this unit, the student will be able to
- define and compare the different budgeting strategies (L2).
- model the cost management as a linear programming problem (L2).
- measure the divisional profitability and decide the appropriate pricing (L2).

Textbook(s):
1. Charles T. Horngren, Srikant M. Datar, George Foster, Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi, 2006.

References:
1. Charles T. Horngren, George Foster, Advanced Management Accounting, Greenwood Publishing, 2001.
2. Robert S Kaplan, Anthony A. Alkinson, Management & Cost Accounting, 1998.
3. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting, Wheeler Publisher, 2004.
4. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book, 2006.

Course Outcomes:

After the successful completion of the course, the students will be able to

- list the basic principles of strategic cost management and define the related terminology (L1).
- plan the project execution process involving technical/nontechnical activities (L4).
- describe the detailed engineering activities and their cost management analysis (L2).
- carry out the cost analysis and profit planning of engineering projects (L5).
- utilize quantitative techniques for optimization of budget allocation (L5).

19EOE752: WASTE TO ENERGY

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This course introduces the basic principles and different technologies of converting waste to energy. Student will be able to appropriately identify the methods and build biomass gasification systems of different capacities depending on application requirements.

Course Objectives:

- to introduce the classification of waste for its usefulness in preparing different fuels
- to familiarize the biomass pyrolysis process and its yield issues
- to acquaint the student with biomass gasification processes and construction arrangements
- to impart the types and principles of biomass combustors
- to familiarize the calorific values and composition of biogas resources

Unit I **8L**

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

Learning Outcomes:

After the completion of this unit, the student will be able to

- distinguish between different types of waste (L1).
- classify the different types of waste for manufacturing different types of fuel (L3). identify the different conversion devices and their applications (L4).

Unit II **8L**

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

Learning Outcomes:

After the completion of this unit, the student will be able to

- classify the different types of pyrolysis methods based on speed (L1).
- describe the different methods of manufacturing charcoal (L2).
- explain the chemical processes involved in the manufacture of pyrolytic oils and gases (L2).

Unit III **8L**

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

Learning Outcomes

After the completion of this unit, the student will be able to

- explain the design, construction and operation of different gasifiers (L2).
- describe the burner arrangement for thermal heating (L2).
- elaborate the gasifier engine arrangement for equilibrium and kinetic considerations (L3).

Unit IV **8L**

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

Learning Outcomes:

After the completion of this unit, the student will be able to

- explain the basic principle of biomass combustors (L2).
- classify different combustors based on their capacity and efficiency (L3).
- describe the construction and operation of fixed bed inclined grate, fluidized bed combustors (L2).

Unit V **10L**

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the properties of biogas (L1).
- elaborate the design, construction and operation of biogas plant (L2).
- classify the different biomass resources and their conversion process (L3).
- distinguish between different biogas plants and identify their applications (L5).

Text Book(s)

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

Course Outcomes:

After the successful completion of the course, the student will be able to

- classify different types of waste for their usefulness in preparing different fuels (L3).
- describe the biomass pyrolysis process and its yield issues (L2).
- outline the different biomass gasification processes and their construction arrangements (L3).
- explain the types and principles of biomass combustors (L2).
- analyze the calorific values and composition of biogas resources (L5).

19EOE758 – C BASED VLSI DESIGN

L T P C
3 0 0 3

Module I **8 Hours**

Introduction: Levels of abstraction – Synthesis – Languages, Design and Technologies – Essential issues in synthesis – Status and future of high-level synthesis. **Architectural Models in Synthesis:** Design styles and target architectures – Combinational logic – Finite state machines – System architecture – Engineering considerations. **Quality Measures**: Relationship between structural and physical designs – Area measures – Performance measures – Other measures.

Module II **8 Hours**

Design Description Languages: Introduction to HDLs – Language models vs architectural styles – Programming language features for HDLs – Hardware-specific HDL features – HDL formats – Modeling guidelines for HDLs. **Design Representation and Transformations**: Design flow in high-level synthesis: An example – HDL compilation – Representation of HDL behavior – Representation of HLS outputs – Transformations.

Module III **8 Hours**

Partitioning: Introduction – Basic partitioning methods – Partitioning in high-level synthesis. **Scheduling**: Problem definition – Basic scheduling algorithms – Scheduling with relaxed assumptions – Other scheduling formulations.

Module IV **8 Hours**

Allocation: Problem definition – Datapath architectures – Allocation tasks – Greedy constructive approaches – Decomposition approaches – Iterative refinement approach. **Design Methodology for High-Level Synthesis:** Basic concepts – Generic synthesis system – System synthesis – Chip synthesis – Logic and sequential synthesis – Physical-design methodology – System database – Component database – Conceptualization environment.

Module V **8 Hours**

System Implementation: Overview of Hercules and Hebe systems. **Experimental Results**: Design experiences: Ethernet co-processor, Digital audio I/O chip, Raster line design, Error correcting codes, Greatest common divisor – Synthesis of benchmark examples.

Text Books:

1. Daniel D Gajski, Nikil D Dutt, Allen C-H Wu and Steve Y-L Lin, "High-Level Synthesis: Introduction to Chip and System Design", Springer Science + Business Media New York, 1st Edition, 1992.
2. David C Ku and Giovanni De Micheli, "High Level Synthesis of ASICs under timing and synchronization constraints", Springer Science + Business Media New York, 1st Edition, 1992.

Reference Books

1. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw Hill, India Edition, 2003.
2. Mike Fingeroff, "High Level Synthesis Blue Book", Mentor Graphics Corporation, 2010.
3. Philippe Coussy and Adam Moraweic, "High-Level Synthesis: From Algorithm to Digital Circuits", Springer, 2008.

Course Outcomes: After successful completion of the course, students will be able to

CO 1 To understand the different levels of abstraction and architectural models
CO 2 To analyze the various representation of hardware description language
CO 3 To interrupt the types of partitioning and scheduling algorithms
CO 4 To analyze the methodologies for resource allocation and synthesis
CO 5 To implement the Hercules/ Hebe systems and benchmarking circuits

19EOE756: WIND ENERGY

L	T	P	C
3	0	0	3

This course gives an overview of key aspects in wind energy engineering. This course covers the most fundamental disciplines of wind energy research such as wind measurements and resource assessment, aerodynamics, wind turbine technology, structural mechanics, materials, financial and electrical systems

Course Objectives:

- To explain the need of wind energy and sitting challenges(L2)
- To find out how the wind power density and the power production can be modeled for an area based on different terrain properties. (L3)
- To learn about financial aspects during the entire lifetime of a wind turbine.(L2)
- To outline the fundamental principle of a wind turbine (L2)
- To discover the forces, act on a wind turbine blade. (L4)

Unit I: **3L**

Introduction to wind energy: pre-requisites, grading policy, math pre-requisites, the need for wind energy, sitting challenges and stakeholder involvement

Learning Outcomes

After completion of this unit the student will be able to

- Recall the theoretical knowledge necessary to complete the course (L1)
- Categorize some of the issues that get addressed in an EIA (L4)
- Recall several types of stakeholders (L1)
- Recognize the two phases of the planning process for a wind farm project (L1)
- Choose the most important environmental issues (L3)

Unit II: **8L**

Wind Resources: wind profiles, wind resource assessment, wind profiles and wind resources, brief introduction with focus on wind energy, wind scanner-remote sensing of wind, wind data analysis

Learning Outcomes:

After completion of this unit, the student will be able to

- Simplify the principle of wind resource assessment (L4)
- Estimate the relevance for wind energy(L5)
- Recognize different remote sensing techniques used for wind energy(L1)
- Express the principle of Doppler shift used in wind lidar (l2)
- Recall the characteristics of a scanning lidar (L1)

Unit III: **8L**

Economy: the cost of wind farms, energy production and revenue, tools for wind energy economics, economics of wind energy – Net Present Value(NPV) , economics of wind energy – Levellised Cost of Energy(LCoE), wind energy technology concepts, wind turbine terminology and components, wind energy technology concepts

Learning Outcomes:

After completion of this unit, the student will be able to

- Appraise simple calculations of a very approximate energy production figure (L5)
- Argue about the importance of revenue in the economics of a wind farm (L4)
- Express the mechanisms of different concepts in energy extraction (L2)
- Appraise the power output for the different concepts (L5)
- Recall the main components of the commercial horizontal-axis wind turbine (L1)
- Recall the main degrees of freedom of the commercial horizontal-axis wind turbine (L1)

Unit IV: 10L

Aerodynamic: power, thrust and optimum rotos, Flow and forces around the wind turbine blade, aerodynamics -1D momentum theory, aerodynamics – rotational theory and velocity triangle , fatigue and mechanical properties of metals, material requirements for wind turbine blades, composite materials for wind turbine blades, stresses in the blade cross section, the weight of a wind turbine blade

Learning Outcomes:

After completion of this unit, the student will be able to

- Recognize how the aerodynamic forces drives the rotor around (L1)
- Appraise the lift on a blade section from an air foil curve (L5)
- Express the use of uniaxial composites in wind turbine blades (L2)
- Estimate the fatigue limit of a composite (L5)
- Express basic mechanical and fatigue properties of metals (L2)
- Appraise the loads and stresses working on a wind turbine blade (L5)

Unit V: 7L

Structural mechanics: structural design of wind turbine blades, beam theory, grid connection of wind power, control of wind turbines and wind power plants, integration of variable wind power generation, wind turbine rotor speed control strategy

Learning Outcomes:

After completion of this unit the student will be able to

- Estimate boundary conditions and loads on beams (L5)
- Simplify the basic principles in structural design (L4)
- Simplify maximum power point tracking (L4)
- Express the control architecture in wind power plants (L2)
- Recognize the four main electrical design concepts for wind turbines (L1)
- Express the electrical layout of a wind power plant (L2)
- Recognize the role of electricity markets, balancing and reserves (L1)

Course Outcomes:

After completion of this course, the student will be able to

- identify the need of wind energy (L1)
- apply basic engineering models for wind speed and determine the annual energy production for a wind turbine. (L3)
- perform simple calculations for assessing wind farm projects and for calculating the cost of energy from wind (L3)
- carry out calculations of thrust and power for a wind turbine (L3)
- define boundary conditions and loads on beams and calculate reactions and internal forces. (L1)

19EOE762 - WEB TECHNOLOGIES

L T P C
3 0 0 3

Module I **8hours**

Introduction to HTML Version5: Basic syntax, HTML document structure, text formatting, images, lists, links, tables, forms, frames, section, article, range and date. **Cascading Style Sheets Version3**: Levels of style sheets, style specification formats, selector forms, font properties, list properties, color properties, alignment of text, background images, span and div tags.

Module II **10 hours**

Introduction to Java Script: Overview of java script, syntactic characteristics, primitives, operator and expression, control statements, arrays, functions, errors in scripts, Document Object Model(DOM), event driven computation, element access in java script, the navigator object. **Dynamic Document with Java Script** : Element positioning, moving elements, changing colors and fonts, dynamic content, locating the mouse cursor, slow movements of elements, dragging and dropping elements.

Module III **8hours**

Introduction to XML: Syntax of XML, document structure, and document type definition, namespaces, XML schemas, document object model, presenting XML using CSS. **Introduction to other XML Technologies**: XLink, XPointer, XQuery and XPath, XQuery and XSLT, XQuery processor and FLWOR expression.

Module IV **8 hours**

Introduction to Servlets: Lifecycle of a servelet, the servlet api, the javax.servelet package, the javax.servlet.http package, handling http request & responses, using cookies, session tracking and security issues and servlets with database connectivity. **Introduction to Model View Controller (MVC):** Architecture, its structure, components.

Module V **8 hours**

Introduction to JSP: The problem with servlet, the anatomy of a JSP page, JSP processing, JSP applications, JSP components, comments, expressions, scriplets, JSTL tag library, JSP database connectivity. **Introduction to Web Servers**: Installing the Java software development kit, tomcat server & testing tomcat, structure of web application, deploying web application, IIS web server, and GWS web server.

Text Book(s)

1. Robert W.Sebesta, Programming the World Wide Web, 4/e, Pearson, 2007.
2. Chris Bates, Web Technologies, 2/e, Wiley, 2002.
3. Jason Hunter, William Crawford, Java Servlet Programming, 2/e, O'Reilly, 2003.

References

1. Dietel and Nieto, Internet and World Wide Web – How to program, PHI/Pearson Education, 2006.
2. Herbert Schildt, JAVA The Complete References, 8/e, McGraw Hill, 2014
3. UttamK.Roy, Web Technologies, Oxford Higher Education publication, 2004.
4. BaiEkedaw, Web Warrior Guide to Web Programmming, Thompson Publications, 2012.

19EOE764 - LINUX PROGRAMMING AND SCRIPTING

L T P C
3 0 0 3

EDA tools run prominently on Linux platforms due to their security features and modular architecture. Information exchange between typical EDA tools typically involves transformation of data. This course exposes students to different commands related to Linux administration and networking. Further the usage of different scripting languages prominently used in conjunction with EDA tools (Perl, TCL/Tk, Python) is introduced.

Course Objectives:

1. To impart the knowledge of Linux operating system and different commands for file and user administration
2. To expose the students to different networking commands used for file transfer, host configuration, IP address look up and remote connection.
3. To acquaint the knowledge of Perl scripting and its utility in transformation of EDA output data
4. To demonstrate the use of TCL commands as an interface to specify constraints and directives to EDA tools
5. To acquaint the knowledge of Python scripting and its utility in transformation of EDA output data

Module I **8 hours**

Linux Basics: Introduction to linux, file system of the linux, general usage of linux kernel & basic commands, Linux users and group, permissions for file, directory and users, searching a file & directory, zipping and unzipping concepts.

Module II **8 hours**

Linux Networking: Introduction to networking in Linux, network basics & tools, file transfer protocol in Linux, network file system, domain naming services, dynamic hosting configuration protocol & network information services.

Module III **8 hours**

Perl Scripting: Introduction to Perl scripting, working with simple values, lists and hashes, loops and decisions, regular expressions, files and data in Perl scripting, references &subroutines, running and debugging Perl, modules, object-oriented Perl.

Module IV **8 hours**

Tcl/tk Scripting: Tcl fundamentals, string and pattern matching, tcl data structures, control flow commands, procedures and scope, evel, working with Unix, reflection and debugging, script libraries, tk fundamentals, tk by examples, the pack geometry manager, binding commands to x events, buttons and menus, simple tk widgets, entry and listbox widgets focus, grabs and dialogs.

Module V **8 hours**

Python Scripting: Introduction to python, using the python interpreter, more control flow tools, data structures, modules, input and output, errors and exceptions, classes, brief tour of the standard library.

Text Books

1. Guido van Rossum and Fred L. Drake Jr., Python Tutorial
2. Brent Welch, Practical Programming in Tcl and Tk, Updated for Tcl 7.4 and Tk 4.0
3. David Till, Teach Yourself Perl 5 in 21 days
4. Red Hat Enterprise Linux 4: System Administration Guide Copyright 2005 Red Hat, Inc

Course Outcomes

Upon successful completion of the course, the student will be able to

1. demonstrate the use of Linux commands for managing files, directories and users
2. configure linux system for providing network connections, DHCP, DNS, FTP services
3. write PERL scripts for transforming output data of EDA tools
4. write appropriate TCL commands for specifying constraints and driving EDA tools
5. write python code for processing output data of automation tools

19EEC792: TECHNICAL SEMINAR

L	T	P	C
0	0	4	2

Each student shall survey a technical topic related to a chosen specialization and prepare/submit a report in a specified format. Each student has to prepare a power point presentation on a selected technical topic with a novelty and get it evaluated by the faculty assigned for this purpose.

19EEC726: ADVANCED VLSI DESIGN LABORATORY

L	T	P	C
0	0	4	2

This laboratory course introduces the Semicustom and full custom IC design methodologies, and their application for designing circuits and systems for high performance and low power applications. The first part covers Backend design tools and methodologies, the second part covers Semicustom design tools and methodologies, and the third part covers circuit design techniques for high performance and low power CMOS design.

Course Objectives

- To familiarize the basic principles of CMOS circuit design and layout design, and verify the performance metrics of Combinational logic (basic and universal logic gates, adders), Sequential logic (Flip Flops and Registers)
- To familiarize the concepts of Semicustom design flow and Hardware description languages (HDL), and to design and implement Combinational and Sequential circuits.
- To introduce low power design methodologies and topologies, to design and analyze Combinational and Sequential circuits for low power.
- To introduce design methodologies and topologies for high performance, to design and analyze Combinational and Sequential circuits for high performance.

Experiments shall be carried out using Xilinx/Cadence Tools

1. Part-I: Backend Design
   Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of CMOS Inverter, NAND Gate, OR Gate, Flip Flops, Register Cell, Half Adder, Full Adder Circuits

2. Part-II: Semicustom Design
   HDL Design Entry/ Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power Analysis of Medium Scale Combinational, Sequential Circuits

3. Part-III: High Speed/Low Power CMOS Design
   Designing combinational/sequential CMOS circuits for High Speed
   Designing combinational/sequential CMOS circuits for Low Power

Course Outcomes:

After successful completion of the course, the student will be able to

- design and analyze Static and Dynamic CMOS circuits (L1).
- understand the timing and power dissipation components of Combinational and Sequential circuits (L2).
- design and verify the functionality of digital circuits and systems, with the help of HDL based design flow developed for ASIC design (L2).
- explore DFT test architectures and implement circuits with DFT (L3).
- understand and implement static timing analysis of Sequential circuits (L3).
- explore power estimation techniques for Combinational and Sequential circuits (L4).
- understand and implement low power architectures and algorithms for digital systems (L5).
- explore critical path balancing techniques and to design circuits for high performance with acceptable power dissipation limits(L5).

19EEC728: IC DESIGN LABORATORY

L	T	P	C
0	0	4	2

Course Objectives:

- To provide hands-on experience in designing analog and digital building blocks, which are extensively used in standard integrated circuits(ICs).
- Student should familiarize with the analog and digital IC design flow.
- Student should familiarize with the tools required to design analog and digital ICs such as Cadence, Synopsys, Xilinx, Matlab etc....

Part-I: Design/Simulation of other analog building blocks

a. Operational Amplifiers
b. Bandgap reference circuits
c. Oscillators
d. PLLs
e. Switched capacitor circuits

Part-II: Mini Projects involving MATLAB Simulation, Verilog Implementation and ASIC implementation of

f. Unpipelined MIPS Processor
g. Pipelined MIPS Processor
h. FIR Filter/IIR Filter/FFT Implementation in Verilog
i. Communication Controllers
j. Arithmetic Circuits
k. Sequential CORDIC System/ Pipelined CORDIC System

Course Outcomes:

After successful completion of the course, the student will be able to

- Describe and explain the operation of fundamental building blocks in analog IC design.
- Describe and explain the operation of fundamental building blocks in digital IC design.
- Differentiate between analog and digital IC design flow. Design basic building blocks in analog and digital ICs.
- Use tools to design analog and digital ICs such as Cadence, Synopsys, Xilinx etc.…

19EEC891: PROJECT WORK – I

L	T	P	C
0	0	26	13

Each student is required to submit a report of first part of project work i.e. about the problem definition, literature review and methodology to be adopted including experiments and tests to be performed on topic of project as per the guidelines decided by the department. The project work is to be evaluated through Presentations and Viva-Voce during the semester end.

19EEC892: PROJECT WORK – II

L	T	P	C
0	0	26	13

Each student is required to submit a detailed project report about the work on topic of project as per the guidelines decided by the department. The project work is to be evaluated through Presentations and Viva- Voce during the semester and Final evaluation will be done at the end of semester as per the guidelines decided by the department from time to time. The candidate shall present/publish one paper in national/international conference/seminar/journal of repute. However, candidate may visit research labs/institutions with the due permission of chairperson on recommendation of supervisor concerned.

HSMCH102 - UNIVERSAL HUMAN VALUES 2: UNDERSTANDING HARMONY

L T P C
2 1 0 3

Human Values Courses: During the Induction Program, students would get an initial exposure to human values through Universal Human Values – I. This exposure is to be augmented by this compulsory full semester foundation course.

Course Objectives:

1. Development of a holistic perspective based on self- exploration about themselves (human being), family, society and nature/existence.
2. Understanding (or developing clarity) of the harmony in the human being, family, society and nature/existence
3. Strengthening of self-reflection.
4. Development of commitment and courage to act.

COURSE TOPICS: The course has 28 lectures and 14 practice sessions in 5 modules:

Module 1: Course Introduction - Need, Basic Guidelines, Content and Process for Value Education

1. Purpose and motivation for the course, recapitulation from Universal Human Values-I.
2. Self-Exploration–what is it? - Its content and process; 'Natural Acceptance' and Experiential Validation- as the process for self-exploration.
3. Continuous Happiness and Prosperity- A look at basic Human Aspirations
4. Right understanding, Relationship and Physical Facility- the basic requirements for fulfilment of aspirations of every human being with their correct priority.
5. Understanding Happiness and Prosperity correctly- A critical appraisal of the current scenario
6. Method to fulfil the above human aspirations: understanding and living in harmony at various levels.

Include practice sessions to discuss natural acceptance in human being as the innate acceptance for living with responsibility (living in relationship, harmony and co-existence) rather than as arbitrariness in choice based on liking-disliking.

Module 2: Understanding Harmony in the Human Being - Harmony in Myself!

1. Understanding human being as a co-existence of the sentient 'I' and the material 'Body'.
2. Understanding the needs of Self ('I') and 'Body' - happiness and physical facility.
3. Understanding the Body as an instrument of 'I' (I being the doer, seer and enjoyer).
4. Understanding the characteristics and activities of 'I' and harmony in 'I'.
5. Understanding the harmony of I with the Body: Sanyam and Health; correct appraisal of Physical needs, meaning of Prosperity in detail.
6. Programs to ensure Sanyam and Health.

Include practice sessions to discuss the role others have played in making material goods available tome. Identifying from one's own life.

Differentiate between prosperity and accumulation. Discuss program for ensuring health vs dealing with disease

Module 3: Understanding Harmony in the Family and Society- Harmony in Human-Human Relationship

1. Understanding values in human-human relationship; meaning of Justice (nine

universal values in relationships) and program for its fulfilment to ensure mutual happiness; Trust and Respect as the foundational values of relationship
2. Understanding the meaning of Trust; Difference between intention and competence
3. Understanding the meaning of Respect, Difference between respect and differentiation; the other salient values in relationship
4. Understanding the harmony in the society (society being an extension of family): Resolution, Prosperity, fearlessness (trust) and co-existence as comprehensive Human Goals
5. Visualizing a universal harmonious order in society- Undivided Society, Universal Order- from family to world family.

Include practice sessions to reflect on relationships in family, hostel and institute as extended family, real life examples, teacher-student relationship, goal of education etc. Gratitude as a universal value in relationships. Discuss with scenarios. Elicit examples from students' lives.

Module 4: Understanding Harmony in the Nature and Existence - Whole existence as Coexistence

1. Understanding the harmony in the Nature
2. Interconnectedness and mutual fulfilment among the four orders of nature-recyclability and self-regulation in nature.
3. Understanding Existence as Co-existence of mutually interacting units in all-pervasive space.
4. Holistic perception of harmony at all levels of existence.
5. Include practice sessions to discuss human being as cause of imbalance in nature (film "Home" can be used), pollution, depletion of resources and role of technology etc.

Module 5: Implications of the above Holistic Understanding of Harmony on Professional Ethics

1. Natural acceptance of human values
2. Definitiveness of Ethical Human Conduct
3. Basis for Humanistic Education, Humanistic Constitution and Humanistic Universal Order
4. Competence in professional ethics: a. Ability to utilize the professional competence for augmenting universal human order b. Ability to identify the scope and characteristics of people friendly and eco-friendly production systems, c. Ability to identify and develop appropriate technologies and management patterns for above production systems.
5. Case studies of typical holistic technologies, management models and production systems
6. Strategy for transition from the present state to Universal Human Order:
7. At the level of individual: as socially and ecologically responsible engineers, technologists and managers
8. At the level of society: as mutually enriching institutions and organizations
9. Sum up.

Include practice Exercises and Case Studies will be taken up in Practice (tutorial) Sessions e.g. To discuss the conduct as an engineer or scientist etc.

READINGS:

Text Book

1. Human Values and Professional Ethics by R R Gaur, R Sangal, G P Bagaria, Excel Books, New Delhi, 2010

Reference Books

1. Jeevan Vidya: EkParichaya, A Nagaraj, Jeevan Vidya Prakashan, Amarkantak, 1999.
2. Human Values, A.N. Tripathi, New Age Intl. Publishers, New Delhi, 2004.
3. The Story of Stuff (Book).
4. The Story of My Experiments with Truth - by Mohandas Karamchand Gandhi.
5. Small is Beautiful - E. F Schumacher.
6. Slow is Beautiful - Cecile Andrews
7. Economy of Permanence - J C Kumarappa
8. Bharat Mein Angreji Raj - PanditSunderlal
9. Rediscovering India - by Dharampal
10. Hind Swaraj or Indian Home Rule - by Mohandas K. Gandhi
11. India Wins Freedom - Maulana Abdul Kalam Azad
12. Vivekananda - Romain Rolland (English)
13. Gandhi - Romain Rolland (English)

MODE OF CONDUCT (L-T-P-C 2-1-0-3 or 2L:1T:0P 3 credits): Lectures hours are to be used for interactive discussion, placing the proposals about the topics at hand and motivating students to reflect, explore and verify them.

Tutorial hours are to be used for practice sessions.

While analysing and discussing the topic, the faculty mentor's role is in pointing to essential elements to help in sorting them out from the surface elements. In other words, help the students explore the important or critical elements.

In the discussions, particularly during practice sessions (tutorials), the mentor encourages the student to connect with one's own self and do self- observation, self-reflection and self-exploration.

Scenarios may be used to initiate discussion. The student is encouraged to take up "ordinary" situations rather than" extra-ordinary" situations.

Such observations and their analyses are shared and discussed with other students and faculty mentor, in a group sitting.

Tutorials (experiments or practical) are important for the course. The difference is that the laboratory is everyday life, and practical are how you behave and work in real life. Depending on the nature of topics, worksheets, home assignment and/or activity are included. The practice sessions (tutorials)would also provide support to a student in performing actions commensurate to his/her beliefs. It is
intended that this would lead to development of commitment, namely behaving and working based on basic human values.

It is recommended that this content be placed before the student as it is, in the form of a basic foundation course, without including anything else or excluding any part of this content. Additional content may be offered in separate, higher courses.

This course is to be taught by faculty from every teaching department, including HSS faculty.

Teacher preparation with a minimum exposure to at least one 8- day FDP on Universal Human Values is deemed essential.

ASSESSMENT:
This is a compulsory credit course. The assessment is to provide a fair state of development of the student, so participation in classroom discussions, self-assessment, peer assessment etc. will be used in evaluation.

Example:
Assessment by faculty mentor: 10 marks
Self-assessment: 10 marks
Assessment by peers: 10 marks
Socially relevant project/Group Activities/Assignments: 20 marks Semester End Examination: 50 marks
The overall pass percentage is 40%. In case the student fails, he/she must repeat the course.

OUTCOME OF THE COURSE:

By the end of the course, students are expected to become more aware of themselves, and their surroundings (family, society, nature); they would become more responsible in life, and in handling problems with sustainable solutions, while keeping human relationships and human nature in mind.

They would have better critical ability. They would also become sensitive to their commitment towards what they have understood (human values, human relationship and human society). It is hoped that they would be able to apply what they have learnt to their own self in different day-to-day settings in real life, at least a beginning would be made in this direction.

This is only an introductory foundational input. It would be desirable to follow it up by
a) faculty-student or mentor-mentee programs throughout their time with the institution
b) Higher level courses on human values in every aspect of living. E.g. as a professional

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