GITAM
(DEEMED TO BE UNIVERSITY)
(Estd. u/s 3 of the UGC Act, 1956)
BENGALURU ❋ HYDERABAD ❋ VISAKHAPATNAM
NAAC Accredited with A+ Grade

REGULATIONS AND SYLLABUS

of

Master of Technology

in

Embedded Systems

(w.e.f. 2019-20 admittedbatch)

A University Committed to Excellence

M.Tech. in Embedded Systems
REGULATIONS
(w.e.f. 2019-20 admitted batch)

1. ADMISSION

Admission into M.Tech. in Embedded Systems program of GITAM (Deemed to be University) is governed by GITAM admission regulations.

2. ELIGIBILITYCRITERIA

2.1 A pass in B.E./B.Tech. /AMIE in ECE / EEE / EIE / Instrumentation / CSE / IT or its equivalent.

2.2 Admissions into M.Tech. will be based on the following:

(i) Score obtained in GAT (PG), if conducted.
(ii) Performance in Qualifying Examination /Interview.
(iii) Candidates with valid GATE score shall be exempted from appearing for GAT(PG).

2.3 The actual weightage to be given to the above items will be decided by the authorities at the time of admissions.

3. CHOICEBASEDCREDITSYSTEM

3.1 Choice Based Credit System (CBCS) was introduced with effect from 2015-16 admitted batch and revised with effect from academic year 2019-20 in order to promote:

- Student centered Learning
- Activity based learning
- Students to learn courses of their choice
- Cafeteria approach

3.2 Learning objectives and outcomes are outlined for each course to enable a student to know what he/she will be able to do at the end of the program.

4. STRUCTURE OF THEPROGRAM

4.1 The Program Consists of

i) Core Courses (compulsory) which give exposure to a student in core subjects related area.

ii) Program Electives.

iii) Open Electives

iv) Mandatory and Audit Courses

4.2 Each course is assigned a certain number of credits depending upon the number of contact hours (lectures/tutorials/practical) per week.

4.3 In general, credits are assigned to the courses based on the following contact hours per week per semester.

- One credit for each Lecture / Tutorial hour per week.
- One credit for two hours of Practical per week.

4.4 The curriculum of the four semesters M.Tech. program is designed to have a total of 68 credits for the award of M.Tech. degree

5. MEDIUMOFINSTRUCTION

The medium of instruction (including examinations and project reports) shall be English.

6. REGISTRATION

Every student has to register for the courses in each semester at the time specified in the academic calendar.

7. ATTENDANCEREQUIREMENTS

7.1 A student whose attendance is less than 75% in all the courses put together in any semester will not be permitted to attend the semester-end examination and he/she will not be allowed to register for subsequent semester of study. He/she has to repeat the semester along with his / her juniors.

7.2 However, the Vice-Chancellor on the recommendation of the Principal / Director of the Institute/School may condone the shortage of attendance to the students whose attendance is between 65% and 74% on genuine grounds and on payment of prescribed fee.

8. EVALUATION

8.1 The assessment of the student's performance in a theory course shall be based on two components: Continuous Evaluation (40 marks) and semester-end examination (60 marks).

8.2 A student has to secure a minimum of 40% in any theory course in the two components (ref. 8.1) put together to be declared to have passed the course, subject to the condition that the student must have secured a minimum of 24 marks out of 60 marks (i.e. 40%) in the theory component at the semester-end examination.

8.3 Practical/ Project Work/ Viva voce/ Seminar etc. course are completely assessed under Continuous Evaluation for a maximum of 100 marks, and a student has to obtain a minimum of 40% to secure Pass Grade. Details of Assessment Procedure are furnished below in Table1.

8.4 Audit courses are assessed through continuous evaluation for satisfactory or not satisfactory only. No credits will be assigned.

Table 1: Assessment Procedure

S.No.	Component of Assessment	Marks Allotted	Type of Assessment	Scheme of Evaluation
1	Theory Courses	40 60	Continuous Evaluation Semester-end Examination	i) Thirty (30) marks for mid Semester examinations. Three mid examinations shall be conducted for 15 marks each; performance in best two shall be taken into consideration. ii) Ten (10) marks for Quizzes, Assignments and Presentations. Sixty (60) marks for Semester-end examinations
	Total	100		
2	Practical Courses	100	Continuous Evaluation	i) Fifty (50) marks for regularity and performance, records and oral presentations in the laboratory. Weightage for each component shall be announced at the beginning of the semester. ii) Ten (10) marks for case studies. iii) Forty (40) marks for two tests of 20 marks each (one at the mid-term and the other towards the end of the semester) conducted by the concerned lab teacher.
3	Technical Seminar (II Semester)	100	Continuous Evaluation	Through five periodic seminars of 20 marks each
4	Project Work (III Semester)	100	Continuous Evaluation	i) Forty (40) marks for periodic assessment on originality, innovation, sincerity and progress of the work, assessed by the project supervisor. ii) Thirty (30) marks for mid-term evaluation for defending the project, before a panel of examiners. iii) Thirty (30) marks for final report presentation and viva-voce, by a panel of examiners*.

5	Project Work (IV Semester)	50	Continuous Evaluation	i) Twenty (20) marks for periodic assessment on originality innovation, sincerity and progress of the work, assessed by the project supervisor. ii) Fifteen (15) marks for mid-term evaluation for defending the project, before a panel of examiners*. iii) Fifteen (15) marks for interim report presentation and viva-voce.
		50	Semester-end Examination	Fifty (50) marks for final project report and viva-voce examination assessed by external examiners.
	Total	100		
6	Audit Courses	100	Continuous Evaluation	Audit courses are assessed for PASS or FAIL only. No credits will be assigned to these courses. If a student secures a minimum of 40 out of 100 marks during continuous evaluation, he / she will be declared PASS, else FAIL. PASS grade is necessary to be eligible to get the degree

**Panel of Examiners shall be appointed by the concerned Head of the Department*

9. PROVISION FOR ANSWER BOOK VERIFICATION AND CHALLENGE EVALUATION

9.1 If a student is not satisfied with his/her grade, the student can apply for answer book verification on payment of prescribed fee for each course within one week after announcement of results.

9.2 After verification, if a student is not satisfied with revaluation marks/grade, he/she can apply for challenge valuation within one week after announcement of answer book verification result or two weeks after the announcement of results, which will be valued by two examiners i.e., one Internal and one External examiner in the presence of the student on payment of prescribed fee. The challenge valuation fee will be returned, if the student is successful in the appeal by securing a better grade.

10. SUPPLEMENTARY AND SPECIALEXAMINATIONS

10.1 The odd semester supplementary examinations will be conducted after conducting regular even semester examinations during April/May.

10.2 The even semester supplementary examinations will be conducted after conducting regular odd semester examinations during October/November.

10.3 A student who has secured 'F' Grade in Project work shall have to improve his/her work and reappear for viva-voce after satisfactory completion of work approved by panel of examiners.

10.4 A student who has completed period of study and has "F" grade in final semester courses is eligible to appear for special examination.

11. MASSIVE OPEN ONLINE COURSES(MOOCs)

Greater flexibility to choose variety of courses is provided through Massive Open Online Courses (**MOOCs**) during the period of study. Students without any backlog courses up to first semester are permitted to register for MOOCs in second semester up to a maximum of 6 credits from program elective / open elective/audit courses. However, the Departmental Committee (DC) of the respective campuses has to approve the courses under MOOCs. The grade equivalency will be decided by the respective Board of Studies(BoS).

12. GRADINGSYSTEM

12.1 Based on the student performance during a given semester, a final letter grade will be awarded at the end of the semester in each course. The letter grades and the corresponding grade points are as given in Table2.

Table 2: Grades and Grade Points

Sl.No.	Grade	Grade Points	Absolute Marks
1	O (outstanding)	10	90 and above
2	A+ (Excellent)	9	80 to 89
3	A (Very Good)	8	70 to 79
4	B+ (Good)	7	60 to 69
5	B (Above Average)	6	50 to 59
6	C (Average)	5	45 to 49
7	P (Pass)	4	40 to 44
8	F (Fail)	0	Less than 40
9	Ab (Absent)	0	-

12.2 A student who earns a minimum of 4 grade points (P grade) in a course is declared to have successfully completed the course, and is deemed to have earned the credits assigned to that course, subject to securing a GPA of 5.0 for a Pass in the semester.

13. GRADE POINTAVERAGE

13.1 A Grade Point Average (GPA) for the semester will be calculated according to the formula:

$$GPA = \frac{\Sigma [C \times G]}{\Sigma C}$$

where, C = number of credits for the course,

G = grade points obtained by the student in the course.

13.2 The Cumulative Grade Point Average (CGPA), is calculated using the above formula considering the grades obtained in all the courses, in all the semesters up to that particular semester.

13.3 CGPA required for classification of class after the successful completion of the program is shown in Table 3.

Table 3: CGPA required for Award of Class

Class	CGPA Required
First Class with Distinction	$\geq$ 8.0*
First Class	$\geq$ 6.5
Second Class	$\geq$ 5.5
Pass Class	> 5.0

* In addition to the required CGPA of 8.0 or more, the student must have necessarily passed all the courses of every semester in the first attempt.

14. ELIGIBILITY FOR AWARD OF THE M.Tech. DEGREE

14.1 Duration of the program: A student is ordinarily expected to complete the M.Tech. Program in four semesters of two years. However, a student may complete the program in not more than four years including study period.

14.2 However, the above regulation may be relaxed by the Vice-Chancellor in individual cases for cogent and sufficient reasons.

14.3 A student shall be eligible for award of the M.Tech. Degree if he / she fulfills all the following conditions.

a) Registered and successfully completed all the courses and project works.

b) Successfully acquired the minimum required credits as specified in the curriculum corresponding to the branch of his/her study within the stipulated period.

c) Has no dues to the Institute, Hostels, Libraries, NCC / NSS etc, and

d) No disciplinary action is pending against him /her.

15. DISCRETIONARYPOWER

Notwithstanding anything contained in the above sections, the Vice Chancellor may review all exceptional cases, and give his decision, which will be final and binding.

M.Tech. in Embedded Systems

Department of Electronic & Communication Engineering
Effective from academic year 2019-20 admitted batch

I Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES701	Microcontrollers for Embedded System Design	PC	3	0	0	3
2	19EES703	Advanced Digital System Design using Verilog	PC	3	0	0	3
3	19EES705	Real Time Operating Systems	PC	3	0	0	3
4	19EES7XX	Program Elective I	PE	3	0	0	3
5	19EES7XX	Program Elective II	PE	3	0	0	3
6	19EMC741	Research Methodology and IPR	MC	2	0	0	2
7	19EES721	Embedded C Laboratory	PC	0	0	4	2
8	19EES723	Advanced Digital System Design Laboratory	PC	0	0	4	2
9	19EAC7XX	Audit Course I	AC	2	0	0	0
							21

II Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES702	Advanced Microcontrollers	PC	3	0	0	3
2	19EES7XX	Program Elective III	PE	3	0	0	3
3	19EES7XX	Program Elective IV	PE	3	0	0	3
4	19EES7XX	Program Elective V	PE	3	0	0	3
5	19EOE7XX	Open Elective	OE	3	0	0	3
6	19EES792	Technical Seminar	PC	0	0	4	2
7	19EES722	Embedded System Laboratory	PC	0	0	4	2
8	19EES724	Digital VLSI Design Laboratory	PC	0	0	4	2
9	19EAC7XX	Audit Course II	AC	2	0	0	0
							21

III Semester

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES891	Project Work I	PW	0	0	26	13
							13

IV Semester

S. No	Course Code	Course Title	Category	L	T	P	C
2	19EES892	Project Work II	PW	0	0	26	13
							13

Number of Credits

Semester	I	II	III	IV	Total
Credits	21	21	13	13	**68**

AUDIT COURSES I and II

S.No	Course Code	Course Title	Category	L	T	P	C
1	19EAC741	English For Research Paper Writing	AC	2	0	0	0
2	19EAC742	Disaster Management	AC	2	0	0	0
3	19EAC743	Sanskrit for Technical Knowledge	AC	2	0	0	0
4	19EAC744	Value Education	AC	2	0	0	0
5	19EAC745	Constitution of India	AC	2	0	0	0
6	19EAC746	Pedagogy Studies	AC	2	0	0	0
7	19EAC747	Stress Management by Yoga	AC	2	0	0	0
8	19EAC748	Personality Development through Life Enlightenment Skills	AC	2	0	0	0
9	19EAC750	Developing Soft Skills and Personality	AC	2	0	0	0

OPEN ELECTIVE

S.No	Course Code	Course Title	Category	L	T	P	C
1	19EOE742	Business Analytics	OE	3	0	0	3
2	19EOE746	Operations Research	OE	3	0	0	3
3	19EOE748	Cost Management of Engineering Projects	OE	3	0	0	3
4	19EOE752	Waste to Energy	OE	3	0	0	3

PROGRAM ELECTIVES

Program Elective I

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES741	Embedded Programming in C and C++	PE	3	0	0	3
2	19EES743	Embedded Networks and protocols	PE	3	0	0	3
3	19EES745	Computer Architecture	PE	3	0	0	3

Program Elective II

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES747	Advanced Digital Signal Processing	PE	3	0	0	3
2	19EES749	Advanced Digital Image processing	PE	3	0	0	3
3	19EES751	Operating Systems	PE	3	0	0	3

Program ElectiveIII

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES742	Digital VLSI Design	PE	3	0	0	3
2	19EES744	Fundamentals of Cryptography and Network Security	PE	3	0	0	3
3	19EES746	Robotics and Control	PE	3	0	0	3

Program ElectiveIV

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES748	Neural Networks and Fuzzy Systems	PE	3	0	0	3
2	19EES750	Digital Systems Testing and Testability	PE	3	0	0	3
3	19EES752	CPLD and FPGA Architectures and Applications	PE	3	0	0	3

Program Elective V

S. No	Course Code	Course Title	Category	L	T	P	C
1	19EES754	DSP Processors	PE	3	0	0	3
2	19EES756	Embedded Linux	PE	3	0	0	3
3	19EES758	Fundamentals and Applications of MEMS	PE	3	0	0	3

19EES701: MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

L	T	P	C
3	0	0	3

This course introduces the students, to 8-bit microcontroller and applications. The first unit covers the architecture of 8051microcontrollers. The next two units cover various interfacing techniques and communication buses. The last two units cover PIC microcontroller and design of applications

Course objectives:

- To learn about the 8051 microcontroller fundamentals.
- To acquaint with the programming of 8051.
- To familiar with the communication buses and protocols in microcontrollers.
- To learn about the basics of PIC microcontroller.
- To interface sensors and actuators to develop applications using PIC microcontrollers.

Unit I: Introduction to Microcontroller (8L)

Introduction to concept of microcontroller, comparison of microprocessor and microcontroller, Intel 8051 microcontroller architecture, pin diagram, addressing modes, special function registers

Learning Outcomes:

After completion of this unit the student will be able to

- compare Microprocessors and microcontrollers (L2).
- explain the architecture of 8051 and pin diagram (L2).
- identify general purpose registers and special purpose registers(L3).

Unit II: Microcontrollers and Processor Architecture & Interfacing (9L)

Counters and timers in 8051, timer modes, serial data input, output, serial data modes, interrupts, timer flag interrupt, serial port interrupt, external interrupts, software generated interrupt control, addressing modes, external data moves, code memory, read only data moves, push and pop instruction set of 8051

Learning Outcomes:

After completion of this unit the student will be able to

- relate counters and timers and its use (L2).
- demonstrate addressing modes used in 8051 microcontroller (L2).
- choose the various types of interrupts (L3).

Unit III: Devices and Buses for Device Networks (9L)

I/O devices, device I/O types and examples, synchronous and asynchronous communications from serial devices, UART and HDLC, parallel port devices, I2C, USB, CAN and advanced I/O serial high speed buses, ISA, PCI bus.

Learning Outcomes:

After completion of this unit the student will be able to

- infer the types of I/O devices (L2).
- select the serial buses and parallel buses used in microcontroller (L3).

- define synchronous and asynchronous protocols (L1).

Unit IV: Introduction PIC Microcontroller (**8L)**

General introduction, PIC16f877 architecture, registers, memory organization, addressing modes, instruction set of PIC microcontroller, PIC16f877 peripherals: timers

Learning Outcomes

After completion of this unit the student will be able to

- spell RISC architecture (L1).
- explain the architecture of PIC microcontroller and pin diagram (L2).
- distinguish addressing modes (L4).

Unit V: Applications **(8L)**

Stepper motor control, speed control of AC, DC motors, position control of AC, motors, traffic light controller, control of physical parameters like temp, pressure, flow, level and humidity.

Learning Outcomes:

After completion of this unit the student will be able to

- apply 8 bit microcontrollers to control AC and DC motors(L3).
- build applications of traffic light control (L3).
- develop measurement of physical parameters such as temperature, pressure (L6).

Text Books:

1. Muhammad Ali Mazidi, Janice Mazidi, Rolin, McKinlay,8051Microcontroller and Embedded Systems, 2/e, PearsonEducation,2005.
2. Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy, PIC Microcontroller and Embedded Systems, 2/e, PearsonEducation,2007.

References:

1. Jonathan W. Valvano, Brookes, Cole, Embedded Microcomputer Systems, Real Time Interfacing, Thomas Learning,1999.
2. John B. Peatman, Designing with PIC Microcontrollers, Prentice Hall of India,1998.
3. Raj Kamal, Embedded Systems - Architecture Programming and Design, 2/e, Tata Mcgraw Hill, 2008.
4. Jan Axelson, Embedded Ethernet and Internet Complete, Penram Publications,2003.

Course Outcomes:

After completion of the course, the student will be able to

- understand the basic concepts of 8051 architectures and addressing modes (L1).
- use the instruction set and peripheral programming (L2).
- understand the communication buses and its protocols (L3).
- understand the basic concepts of PIC architecture and addressing modes (L4).
- apply the interfacing concepts with PIC microcontrollers (L5).

19EES703: ADVANCED DIGITAL SYSTEM DESIGN USING VERILOG

L	T	P	C
3	0	0	3

This course introduces the students, to Verilog modeling and design applications with CPLD and FPGA. The first unit covers language constructs and conventions of Verilog. The next two units cover various modeling techniques and hardware required to design digital IC's. The last two units cover design applications with CPLD and FPGA.

Course objectives:

- Understand the basics of the language and its conventions.
- To learn modeling at gate level, behavioral level and dataflow level.
- To model, simulate and synthesize the digital designs using Verilog HDL.
- To describe and realize the functionality of the digital design by using ASM Charts.
- To know architectural features and implementation of digital designs in CPLDs &FPGAs.

Unit I: Introduction to Verilog **(9L)**

Verilog as HDL, levels of design description, concurrency, simulation and synthesis, functional verification, system tasks, programming language interface (PLI), Unit, simulation and synthesis tools, test benches, language constructs and conventions. Gate Level Modeling: Introduction, and gate primitive, other gate primitives, illustrative examples, tri-state gates, array of instances of primitives.

Learning Outcomes:

After completion of this unit the student will be able to

- define language constructs of Verilog (L1).
- illustrate simulation and synthesis (L2).
- demonstrate gate Verilog modeling (L2).

Unit II: Behavioral Modeling **(8L)**

Introduction, operations and assignments, functional bifurcation, initial construct, always construct, examples, assignments with delays, wait construct, multiple always blocks, designs at behavioral level, blocking and non-blocking assignments, case, if, assign, repeat, for-loop.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate behavioral Verilog modeling (L2).
- classify blocking and non-blocking assignments (L2).
- apply control loops such as for and decision statements such as if -else (L3).

Unit III: Introduction to Programmable Logic Devices **(9L)**

Brief overview of programmable logic devices, simple programmable logic devices, complex programmable logic devices, field-programmable gate arrays.
Design examples: BCD to 7-segment display decoder, BCD adder, 32-bit adders, traffic light controller, state graphs for control circuits, score board and controller.

Learning Outcomes:

After completion of this unit the student will be able to

- outline CPLD and FPGA as programmable devices (L2).
- build combinational circuit models with Verilog (L3).
- develop FSM charts using Verilog (L3).

Unit IV: Digital Design with State Machine Charts (8L)

State machine charts, derivation of SM charts, realization of SM charts, implementation of the dice game, alternative realizations for SM charts using micro programming, linked state machines.

Learning Outcomes:

After completion of this unit the student will be able to

- evaluate SM chart for dice game(L5).
- analyze linked state machines (L4).
- develop SM charts using microprogramming (L3).

Unit V: Designing with FPGAs and CPLDs (8L)

Xilinx 3000 series FPGAS, designing with FPGAS, using a one- hot state assignment, Altera complex programmable logic devices. Verilog Models: Static RAM memory, a simplified 486 bus model, UART design.

Learning Outcomes:

After completion of this unit the student will be able to

- experiment with Xilinx 3000 series FPGAS (L4).
- analyze one-hot state assignment (L4).
- develop memory and UART Verilog models (L3).

Text Books:

1. T.R. Padmanabhan, B. BalaTripura Sundari, Design through Verilog HDL, Wiley Student Edition, IEEE Press,2004.
2. Charles H Roth, Digital Systems Design using VHDL, 2/e, Thomson Publications,2014.

References

1. Stephen. Brown and Zvonko Vranesic, Fundamentals of Logic Design with Verilog, Tata Mcgraw Hill, 2005.
2. J. Bhasker, A Verilog HDL Premier, Prentice Hall of India,1999.
3. Zainalabedin Navabi, Verilog system design, Springer Science,2005.
4. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, Pearson,2011.

Course Outcomes:

After completion of the course, the student will be able to

- understand Verilog language structure and levels of design description (L2)
- develop HDL code for digital system designs (L1)
- use Verilog coding techniques for describing actual hardware components (L3)
- implement and test design on the target CPLD's & FPGA's (L2)
- develop different digital solutions ranging from signal processing, data manipulation, electronic instrumentation, control, and telecommunications to consumer electronics (L5)

19EES705: REAL TIME OPERATINGSYSTEMS

L	T	P	C
3	0	0	3

This course introduces the student about the importance of RTO's in an embedded system. The first unit covers different types of operating systems. The next three units cover basic concepts of RTO's and IPC synchronization techniques. The last two units cover resource management in RT Linux.

Course Objectives:

- To study about the difference between OS, RTOS and hardware organization.
- To study about the Basic concepts of RTOS.
- To know the Scheduling Algorithms and scheduling criteria in RTOS.
- To know the inter process communication between tasks and processes.
- To study about different types of RTOS like RT Linux and Vx Works.

Unit I: Introduction **(8L)**

Introduction to operating system, different types of OS, OS services, computer hardware organization: ALU, memory, pipelining, registers, serial ports, BIOS and BOOT process, multi-threading concepts, processes, threads

Learning Outcomes:

After completion of this unit the student will be able to

- compare the features of general purpose OS and RTO's(L2).
- explain the BIOS and BOOT process in RTO's (L2).
- illustrate processes and multi threading (L2).

Unit II: Basics of real-time concepts **(8L)**

Introduction to real time systems, types of real time systems, differences between OS and RTOs, task and task states, shared resources, critical section of code, task switching, real-time design issues, examples, and hardware considerations: logic states, CPU, memory, I/O, architectures, RTOs building blocks, real-time kernel.

Learning Outcomes:

After completion of this unit the student will be able to

- explain tasks and its states in RTO's(L2).
- choose the types of RTO's (L3).
- demonstrate real time kernel (L2).

Unit III: Process Management **(8L)**

Concepts, scheduling, IPC, RPC, CPU Scheduling, scheduling criteria, scheduling algorithms. Threads: Multi-threading models, threading issues, thread libraries, synchronization Mutex: creating, deleting, prioritizing Mutex.

Learning Outcomes:

After completion of this unit the student will be able to

- apply the knowledge of scheduling algorithm suitable for the application(L3).

- choose Multi-threading models in RTO's (L3).
- outline the process of mutex creation (L2).

Unit IV: Inter-process communication (9L)

Buffers, mailboxes, queues, semaphores, deadlock, priority inversion, Pipes. Memory Management: process stack management, run-time buffer size, swapping, overlays, block/page management, replacement algorithms

Learning Outcomes:

After completion of this unit the student will be able to

- compare IPC techniques used in RTO's (L3).
- explain the concept of priority inversion in RTO's (L2).
- infer memory management done in RTO's (L2).

Unit V: Case Study: RT Linux (9L)

Process management, scheduling, interrupt management, and synchronization, Vx works: memory managements task state transition, diagram, pre-emptive priority, scheduling, context switches, semaphore, binary mutex, counting.

Learning Outcomes:

After completion of this unit the student will be able to

- discover process and interrupt management in RT Linux (L4).
- apply the knowledge of context switching in RT Linux (L3).
- explain the selection binary semaphore, counting semaphore or mutex (L2).

Text Books:

1. J. J. Labrosse, Micro C/OS-II: The Real-Time Kernel, 2/e, CMP Books,2002.
2. Herman B, Real-Time and Embedded Guide,2001.
3. Philips A. Laplander, Real-Time System Design and Analysis, 4/e, Wiley,2011.
4. Doug Abbott, Linux for Embedded and Real-Time Applications, 3/e, Newness,2011.

References

1. Richard Stevens, Advanced UNIX Programming, 3/e, Wiley,2013.
2. Wind River Systems, VX Works Programmers Guide, Wind River Systems,1993.

Course Outcomes:

After completion of the course, the student will be able to

- understand about difference between OS and RTOS (L1).
- understand about key Real-Time Operating System terms and Concepts (L2).
- write programs of an embedded system with scheduling the tasks and execute (L3).
- understand about different types inter process communication mechanisms and memory management (L4).
- understand different types of RTOS like RT Linux and Vx works (L5).

19EES741: EMBEDDED PROGRAMMING IN C AND C++

L	T	P	C
3	0	0	3

This course introduces the students, to develop programs for embedded systems with embedded C and C++. The first unit covers Introduction to C, data types and super loop architecture. The next two units cover creating delays and design of UART Protocol. The last two units covers embedded C++ programming and OOP's concept

Course Objectives:

- To show how simple C programs can be developed and tested using the software tools
- To learn the techniques for reading port pins and working with mechanical switches
- Techniques to create more flexible operating systems for processors.
- To learn the Basics of C++
- To learn the Basics of Embedded C++ and how simple C++ programs developed and tested.

Unit I: Programming in C (8L)

Introduction to C - data types, structures, functions, arrays, pointers, strings, hello world program, super loop architecture, delay function, controlling the port pins, reading switches.

Learning Outcomes:

After completion of this unit the student will be able to

- explain data types in C language and functions of C(L2).
- show to control of input and output ports (L2).
- develop software delay function with C (L3).

Unit II: Embedded C 8L

Selection of processors, programming language, operating system, object-oriented programming with C, the project header (main.h), the port header (port.h) meeting real time constraints, creating hardware delays using timer.

Learning Outcomes:

After completion of this unit the student will be able to

- select the processor required for an embedded system(L1).
- demonstrate of project header files to meet real time constraint (L2).
- develop hardware delay functions with timers in C (L3).

Unit III: Multi-State Systems and Function Sequences in C (9L)

Introduction- implementing a multi-state (timed) system, traffic light sequencing, implementing a multi-state (input/timed) system, controller for a washing machine using the serial interface, basic RS-232 protocol, asynchronous data transmission and baud rates, flow control, the software architecture, using the on-chip UART for RS- 232 communications.

Learning Outcomes:

After completion of this unit the student will be able to

- illustrate multi stage and multi state system (L2).
- make use of Rs-232 protocol (L3).
- compile UART for RS- 232 communications in C (L6).

Unit IV: Programming in C++ **(9L)**

C++ initiation, the main() function, C++ comments, C++ preprocessor, IO stream file, header filenames, C++ output, statements, functions, user defined functions, dealing with data, simple variables, floating-point numbers, C++ arithmetic operators, pointers, arrays, and pointer arithmetic, loops and relational expressions, function overloading, objects and classes.

Learning Outcomes:

After completion of this unit the student will be able to

- how to write program in C++ (L1).
- explain predefined and user defined functions with C++ (L2).
- illustrate objects, classes and operator overloading in C++(L2).

Unit V: Embedded C++ **(8L)**

Introduction, conceptual and physically realizable objects, real objects, object classes, encapsulation, abstract classes, dynamic memory allocation, class hierarchies, inheritance, multiple inheritance, polymorphism.

Learning Outcomes:

After completion of this unit the student will be able to

- show the dynamic memory allocation in Embedded C++ (L2).
- relate classes and abstract classes (L1).
- apply inheritance and polymorphism (L3).

Text Books:

1. Michael J. Pont, Embedded C Addison Wesley, Pearson Education Limited,2002.
2. Dr. Jayantha Katupitiya, Mr. Kim Bentley, Interfacing with C++ - Programming Real World Applications, Pringer Verlag Berlin Heidelberg,2006.

References

1. Matthew Wilson, Imperfect C++ Practical Solutions for Real-Life programming, Addison Wesley Professional2004.
2. Stephen Prata, C++Primer Plus Sams Publishing,2005.
3. Michael Barr, Programming Embedded Systems in C and C++,O'Reilly,1999.
4. Jean Labrosse, Jack Ganssle, Tammy Noergaard, Robert Oshana, ColinWalls, Keith Curtis, Jason Andrews, David J. Katz, Rick Gentile, Kamal Hyder, Bob Perrin, Embedded Software, Elsevier, 2008.
5. Alan Holub, Compiler Construction in C, Prentice Hall ofIndia,2005.

Course Outcomes:

After completion of the course, the student will be able to

- write simple C programs and tested using software tools (L1).
- create executable code for an embedded processor on a desktop PC (L2).
- create a simple but functional code framework for an embedded Applications (L3).
- understand basics of C++ (L5).
- understand basics of Embedded C++ and Programming in Embedded C++ (L4).

19EES743: EMBEDDED NETWORKS AND PROTOCOLS

L	T	P	C
3	0	0	3

This course introduces the students, to embedded networking and its required protocols. The first unit covers the importance of controller area network bus. The next two units cover basics of Ethernet, embedded Ethernet and protocols suite like UDP and TCP. The last two units cover industrial networking protocols and wireless networking concepts.

Course Objectives:

- To study the general concepts of bus access and arbitration, error processing and management of CAN2.0A and CAN 2.0B.
- To know Elements of a network and building a network.
- To study Embedded Ethernet, exchanging messages using UDP and TCP.
- To develop Industrial networking protocol.
- To acquire knowledge on RF communication.

Unit I: Introduction to CAN **(9L)**

The CAN bus, general concepts of bus access and arbitration, error processing and management, from concept to reality, patents, licenses and certification, CAN protocol: 'ISO 11898-1', content of the different ISO/OSI layers of the CAN bus, compatibility of CAN 2.0A and CAN 2.0B.

Learning Outcomes:

After completion of this unit the student will be able to

- what is the need for CAN bus in embedded systems(L1).
- classify layers in CAN protocol (L2).
- distinguish the CAN 2.0A and CAN 2.0B (L4).

Unit II: Ethernet basics **(9L)**

Elements of a network, inside Ethernet, building a network: hardware options, cables, connections and network Speed, design choices: selecting components, Ethernet controllers, using the internet in local and internet communications, inside the internet protocol.

Learning Outcomes:

After completion of this unit the student will be able to

- tell the elements inside Ethernet (L1).
- select the components and cables required for Ethernet (L1).
- infer internet protocol (L2).

Unit III: Embedded Ethernet **(8L)**

Exchanging messages using UDP and TCP, serving web pages with dynamic data, serving web pages that respond to user input, email for embedded systems, using FTP, keeping devices and network secure.

Learning Outcomes

After completion of this unit the student will be able to

- plan to service the data using UDP or TCP protocol (L3).
- summarize the use of FTP(L2).
- identify the devices for network security (L3).

Unit IV: Industrial networking protocol (8L)

LIN–local inter connect network, basic concept of the LIN2.0 protocol, fail-safe SBC, gateways, managing the application layers, safe-by-wire, safe-by-wire plus, audio-video buses, I2C bus, D2B (domestic digital) bus, MOST (media oriented systems transport) bus, IEEE 1394 bus or 'Fire wire', profibus.

Learning Outcomes:

After completion of this unit the student will be able to

- what is the need for profibus in industries (L1).
- explain the LIN 2.0 protocol(L1).
- distinguish between I2C, IEEE 394, LIN, fire wire buses (L4).

Unit V: RF communication (8L)

Radio-frequency communication: internal and external, remote control of opening parts, PKE (passive keyless entry) and passive go, TPMS (tyre pressure monitoring systems), wireless networks, GSM, Bluetooth, IEEE 802.11x - NFC (near-field communication).

Learning Outcomes:

After completion of this unit the student will be able to

- spell the radio frequency communication in remote control(L1).
- outline tyre pressure monitoring using RF(L2).
- select either Bluetooth or GSM or NFC required for the wireless networks based on the application (L3).

Text Books:

1. Dominique Paret Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire, John Wiley and Sons,2007.
2. Jan Axelson, Embedded Ethernet and Internet Complete, Penram publications

References

1. Glaf P.Feiffer, Andrew Ayre, Christian Keyold, "Embedded networking with CAN and CAN open". Embedded System Academy,2005.
2. Gregory J. Pottie, William J. Kaiser "Principles of Embedded Networked Systems Design",2/e, Cambridge University Press,2005.

Course Outcomes:

successful completion of the course, the student will be able to

- understand the CAN bus and compatibility of CAN 2.0A and CAN 2.0B (L1).
- understand the performance characteristics and transient response of MEMS structures (L2).
- understand Ethernet basics and design choices (L3).
- realize Industrial networking protocols like LIN (L4).
- understand current trends in RF communication (L5).

19EES745: COMPUTERARCHITECTURE

L	T	P	C
3	0	0	3

This course introduces the students, to the insight details of the architecture of a computer. The first unit covers the how the instruction set is designed with different addressing modes. The next two units cover the concept of pipelining and memory organization. The last two units cover multi processor design and parallelism and how the different memories like cache, main, virtual memory works.

Course Objectives:

- To know the principles involved design of instruction set
- To understand the implementation and its complications.
- To the importance of cache, main and virtual memory.
- To know the importance of thread level parallelism in multi processor design.
- To understand the different storage devices and communication with I/O devices

Unit I: Fundamentals of Computer Design **(9L)**

Technology trends, cost measuring and reporting, performance quantitative principles of computer design. Instruction set principles and examples: Classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set, instruction for control, encoding an instruction set.

Learning Outcomes:

After completion of this unit the student will be able to

- show the quantitative principles of computer design (L1).
- classifying instruction set (L2).
- explain Instruction set principles(L2).

Unit II: Pipelining **(8L)**

Introduction, the major hurdle of pipelining: pipeline hazards, how is pipelining implemented? What makes pipelining hard to implement? Extending the MIPS pipeline to handle multi cycle operations. Instruction Level Parallelism: Overcoming hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP, ILP software approach, compiler techniques, static branch protection VLIW approach.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the concept of pipelining and how it is implemented(L2).
- relate the hazards in instruction level parallelism (L2).
- outline VLIW approach and hardware constraints (L2).

Unit III: Memory Hierarchy Design **(9L)**

Introduction, review of the abcs of caches, cache performance, reducing cache miss penalty, reducing miss rate, reducing cache miss penalty or miss rate via parallelism, reducing hit time, main memory and organizations for improving performance, memory technology, virtual memory, protection and examples of virtual memory, basics of virtual machines.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the differences between cache memory and main memory (L2).
- inspect miss penalty or miss rate via parallelism(L4).
- summarize virtual memory and its protection (L2).

Unit IV: Multiprocessors and Thread-Level Parallelism (8L)

Introduction, characteristics of application domains, symmetric shared-memory architectures, performance of symmetric shared-memory multiprocessors, distributed shared-memory architectures, performance of distributed shared-memory multiprocessors, synchronization. Models of memory consistency: an introduction, multithreading, exploiting thread-level parallelism within a processor.

Learning Outcomes:

- compare between the shared memory and distributed memory(L2).
- outline thread-level parallelism within a processor(L4).
- summarize the performance of multiprocessors (L2).

Unit V: Storage Systems (8L)

Introduction, types of storage devices, buses-connecting I/O devices to CPU/memory, reliability, availability, and dependability, raid, redundant arrays of inexpensive disks, errors and failures in real systems, I/O performance measures, designing an I/O system in five easy pieces.

Learning Outcomes:

After completion of this unit the student will be able to

- compare types of storage devices (L2).
- interpret I/O devices interfacing to memory(L2).
- summarize the errors and failures in real time systems with memory(L2).

Text Book

1. John L, Hennessy & David A Patterson, Computer Architecture a quantitative approach, 3/e, Morgan Kuffman, 2011.

References

1. John L, Hennessy & David A Patterson, Computer Architecture a quantitative approach, 4/e, MorganKuffman,2012.
2. Kai Hwang and A. Briggs, Computer Architecture and Parallel Processing, International Edition, McGrawHill,2011.
3. Dezso Sima, Terence Fountain, Peter Kacsuk, Advanced Computer Architecture, Pearson Education,2011.

Course Outcomes

After successful completion of the course, the student will be able to

- understand the instruction set design and addressing modes (L1).
- understand the advantages of pipelining, hazards and VLIW (L2).
- understand how the main memory, cache memory and virtual memory effects the performance (L3).
- understand the effects of thread level parallelism (L4).
- understand the problems encountered in interfacing different types of memory to I/O devices (L5).

19EES747: ADVANCED DIGITAL SIGNALPROCESSING

L	T	P	C
3	0	0	3

This course introduces the students, to apply advanced signal processing techniques such as DFT, FFT and wavelet transforms. The first unit covers to understand DFT and FFT signal processing techniques. The next two unit's s covers multirate signal processing and design of filters with DSP. The last two units cover design of adaptive filters using popular LMS and RLS algorithms and estimation of power spectra.

Course Objectives:

- To refresh the basics of digital signal processing.
- To introduce and analyze multi rate signal processing.
- To learn linear prediction and optimum linear filters.
- To study the concepts and applications of adaptive filters.
- To analyze the methods of power spectrum estimation.

Unit I: Introduction **(8L)**

Discrete time Fourier transform, discrete time fourier series, discrete fourier transform (DFT), properties of DFT, computation of DFT, circular convolution and linear convolution using DFT, fast fourier transform (FFT).

Learning Outcomes:

After completion of this unit the student will be able to

- distinguish between DFT and FFT (L4).
- demonstrate properties of DFT(L2).
- classify linear convolution and circular convolution using DFT(L2).

Unit II: Multi rate Digital Signal Processing **(9L)**

Introduction, decimation by a Factor D, interpolation by a factor I, sampling rate conversion by a rational factor I/D, implementation of sampling rate conversion, introduction to time frequency analysis, continuous time wavelet transform, discrete wavelet transform.

Learning Outcomes:

After completion of this unit the student will be able to

- summarize multi rate signal processing (L4).
- demonstrate time frequency analysis (L2).
- explain wavelet transform (L2).

Unit III: Linear Prediction and Optimum Linear Filters **(9L)**

Random signals, correlation functions and power spectra, innovations representation of a stationary random process, forward and backward linear prediction, ARMA lattice-ladder filters, wiener filters for filtering and prediction.

Learning Outcomes:

After completion of this unit the student will be able to

- summarize linear filters (L4).
- demonstrate correlation functions (L2).
- compare forward and backward linear prediction (L2).

Unit IV: Adaptive Filters **(8L)**

Applications of adaptive filters, adaptive direct-form FIR filters, the LMS algorithm, adaptive direct-form FIR filters, and RLS algorithms.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate time frequency analysis (L2).
- explain LMS algorithm (L2).
- illustrate RLS algorithm (L4).

Unit V: Power Spectrum Estimation **(8L)**

Estimation of spectra from finite-duration observations of signals, nonparametric methods for power spectrum estimation, and parametric methods for power spectrum estimation.

Learning Outcomes:

After completion of this unit the student will be able to

- show power spectrum estimation of finite duration signals (L1).
- outline nonparametric methods for power spectrum estimation (L2)
- outline parametric methods for power spectrum estimation (L2).

Text Books:

1. J.G.Proakis, D. G. Manolakis, Digital Signal Processing– Principles, Algorithms, Applications, 4/e, Pearson Education,2007.
2. Sanjit K. Mitra, Digital Signal Processing, A Computer–Based approach, 3/e, Tata Mcgraw Hill, 1998.

References

1. Monsom H.Hayes, Statistical Signal Processing, John Wiley & Sons, INC,2009.
2. Raghuveer M Rao, Ajit S, Bopardikar, Wavelet Transforms: Introduction to Theory and Applications, Pearson Education,2000.

Course Outcomes:

successful completion of the course, the student will be able to

- compute the DTFS and DFT for digital signals (L1).
- understand and apply multirate signal processing (L3).
- find the response of random signals using linear prediction and optimum linear filters (L5).
- understand and apply linear filters in real time applications (L2).
- estimate the power spectrum of signals using parametric and non-parametric methods (L4).

19EES749: ADVANCED DIGITAL IMAGE PROCESSING

L	T	P	C
3	0	0	3

This course introduces the students, to apply advanced image processing techniques such as image sensing and image segmentation etc. The first unit covers about the image representation, sensing and basic operations on image. The next two units cover image enhancement and restoration techniques. The last two units cover image edge and line detection and image classifiers processing.

Course Objectives:

- To refresh the basics of digital image processing.
- To learn the image enhancement techniques of DIP.
- To learn the image restoration techniques of DIP.
- To study the morphological image processing techniques.
- To analyse the methods of image representation.

Unit I: Introduction **(8L)**

Digital image representation, fundamental steps in digital image processing, elements of digital image processing systems, elements of visual perception, a simple image model, image sensing and acquisition, image sampling and quantization, neighborhood of pixels, pixel connectivity, labeling of connected components, distance measures, arithmetic and logic operations, image transformations, perspective transformations.

Learning Outcomes:

After completion of this unit the student will be able to

- tell image model and steps in image processing (L1).
- illustrate image sensing and its acquisition (L2).
- interpret arithmetic and logical operations on image (L2).

Unit II: Image Enhancement **(8L)**

Spatial domain methods, point processing, intensity transformations, histogram processing, spatial filtering, smoothing filters, sharpening filters, image enhancement in the frequency domain, smoothing filters, low pass filtering, sharpening filters, high pass filtering, homomorphic filtering.

Learning Outcomes:

After completion of this unit the student will be able to

- apply low pass filters and high pass filters on image(L3).
- illustrate image histogram processing (L2).
- summarize image filtering techniques (L2).

Unit III: Image Restoration **(9L)**

Model of image degradation/ restoration process, noise models, restoration in presence of noise only- spatial filtering, periodic noise reduction by frequency domain filters, inverse filtering. Image Compression: Fundamentals of compression, image compression model, error free compression, Huffman and LZW coding, lossy predictive coding, transform coding.

Learning Outcomes:

After completion of this unit the student will be able to

- explain image restoration techniques (L2).
- apply image compression techniques (L3).
- demonstrate frequency domain of image processing (L2).

Unit IV: Morphological Image Processing (9L)

Dilation and erosion, opening and closing, boundary extraction, region filling, convex hull, thinning, thickening, skeletons, pruning. Image Segmentation: Detection of discontinuities, line detection, edge detection, edge linking and boundary detection, thresholding, threshold selection on boundary characteristics, region growing, region splitting and merging, use of motion in segmentation.

Learning Outcomes:

After completion of this unit the student will be able to

- select image processing based on boundary, hull or skeleton (L1).
- make use of line detection in image (L3).
- choose thresholding in image segmentation (L3).

Unit V: Image Representation and Description (8L)

Chain codes, polygonal approximations, signatures, skeleton, boundary descriptions, shape numbers, Fourier descriptors, moments, topological descriptors. Image Recognition and Interpretation: Elements of image analysis, pattern and pattern classes, minimum distance classifier, matching by correlation, baye's classifier, neural network training algorithm, structural methods, syntactic recognition.

Learning Outcomes:

After completion of this unit the student will be able to

- illustrate the selection of image descriptors (L2).
- apply image classifiers (L3).
- select structural methods on image processing (L1).

Text Books:

1. Rafael C Gonzalez and Richard E Woods, Digital Image Processing, Pearson Education Asia, New Delhi,2000.
2. B. Chanda, D. Dutta Majumder, Digital Image Processing and Analysis, Prentice Hall of India, NewDelhi,2000.

References

1. Anil K. Jain, Fundamentals of Digital Image Processing, Prentice Hall of India, New Delhi,

Course Outcomes:

After successful completion of the course, the student will be able to

- represent an image in pixel format to do basic DIP operations (L1).
- understand the methods of spatial and frequency domain image enhancement (L3).
- analyze noisy images and implement the image compression methods (L2).
- perform image segmentation using morphological techniques (L3).
- perform image recognition and interpretation using coding techniques(L4).

19EES751: OPERATING SYSTEMS

L	T	P	C
3	0	0	3

This course introduces the students, to need of operating system to control multi processes in a computer. The first unit covers objective of operating system and the building blocks of a computer. The next two units cover process management and memory management by the kernel. The last two units cover the purpose scheduling and various algorithms and file management in OS.

Course Objectives

- To refresh the basics of computer hardware and operating system objectives
- To learn the process states and control in OS.
- To learn the memory management in OS.
- To learn various scheduling algorithms used in OS.
- To file management in various operating systems.

Unit I: Computer System and Operating System Overview **(9L)**

Overview of computer system hardware, Instruction execution, I/O function, interrupts, memory hierarchy, I/O communication techniques, operating system objectives and functions, evaluation of operating system, example systems.

Learning Outcomes:

After completion of this unit the student will be able to

- explain hardware in computer (L2).
- illustrate the need for operating system (L3).
- define example systems (L1).

Unit II: Process Description **(8L)**

Process control, process states-process and threads-examples of process description and control. Concurrency: Principles of concurrency, mutual exclusion, software and hardware approaches, semaphores, monitors, message passing, reader's writer's problem. Principles of deadlock: Deadlock prevention, detection and avoidance dining philosopher's problem, example systems.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the process description and control done with OS (L2).
- summarize, software and hardware approaches (L2).
- infer deadlock detection and prevention(L2).

Unit III: Memory Management **(9L)**

Memory Management: Memory management requirements, loading programs into main memory, virtual memory, hardware and control structures, OS software, examples of memory management.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate memory management in OS (L2).
- compare main memory vs virtual memory (L2).
- illustrate examples of memory management(L2).

Unit IV: Uniprocessor Scheduling **(8L)**

Types of scheduling, scheduling algorithms, I/O management and disc scheduling, I/O devices, organization, of I/O function, OS design issues, I/O buffering, disk I/O, disk scheduling policies, examples system.

Learning Outcomes:

After completion of this unit the student will be able to

- choose types of scheduling algorithms in OS (L3).
- demonstrate I/O and memory management scheduling policies (L2).
- illustrate examples systems with scheduling(L2).

Unit V: File Management and Security **(8L)**

Overview of file management, file organization and access, file directories, file sharing, record blocking, secondary storage management, example system. Security: Security threats, protection, intruders, viruses, trusted system, case studies of Linux, UNIX, Windows XP, and VxWorks.

Learning Outcomes:

After completion of this unit the student will be able to

- interpret file organization and file sharing in OS (L2).
- explain the file security in OS (L2).
- compare Linux, UNIX, Windows XP, and VxWorks (L2).

Text Books:

1. Abraham Silberchatz, Peter B, Galvin, Greg Gagne, Operating System Principles, 7/e, John Wiley, 2012.

References

1. Stallings, Operating Systems – Internal and Design Principles, 5/e, Pearson Education,2014
2. Crowley, Operating System A Design Approach, Tata McGraw Hill,2015
3. Andrew S Tanenbaum, Modern Operating Systems, 2/e, Pearson Education,2010

Course Outcomes:

successful completion of the course, the student will be able to

- understand the how the computer hardware works with OS(L1).
- understand the methods of process control with semaphores and deadlock problems(L2).
- understand the loading programs in main memory and virtual memory(L3).
- understand the scheduling algorithms and I/O, memory management(L4).
- differentiate the features in UNIX, Windows XP, and Vx Works(L5).

19EMC741: RESEARCH METHODOLOGY AND IPR

L	T	P	C
2	0	0	2

This course introduces the student, to the fundamentals of research, research process, technical writing and intellectual property rights. Students will be able to use this knowledge to gain interest in their subject area and pursue their career in research.

Course Objectives:

- To familiarize the meaning, objectives and sources of research
- To acquaint the student with the importance and methods of literature review/research ethics
- To impart the knowledge of technical writing for preparing reports, presentations, research proposals, conference/journal publications
- To introduce the terminology and process of obtaining intellectual property rights
- To expose the intricacies in the process of obtaining patent rights

Unit I **5L**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the meaning of a research problem (L2).
- list the different sources of research problem (L1).
- enumerate the different criteria of good research and list the different errors in selecting research problem (L4).
- contrast the different approaches of research (L3).
- compare the different methods for data collection and analysis (L5).

Unit II **5L**

Effective literature studies approaches, analysis Plagiarism, Research ethics.

Learning Outcomes:

After the completion of this unit, the student will be able to

- list and elaborate the different steps of the research process (L1).
- explain the importance of carrying out an effective literature review (L3).
- identify the research gaps from literature review (L4).
- describe the ethical principles to be following during research process and authorship (L2).
- define the terminology and list the methods to avoid being accused of plagiarism (L2).
- list the different types of research misconduct (L5).

Unit III **5L**

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the attributes, reasons and guidelines for effective technical writing (L3).
- contrast between conference paper, technical presentation and journal paper (L2).
- choose a particular research contribution for patenting or journal publication (L4).

- define the terminology related to citation, citation index, h-index etc (L1).

Unit IV **5L**

Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. **International Scenario**: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the codes and standards in building intellectual property rights(L3).
- list the subject, importance and requirements for of patentability(L5).
- explain the process of patenting and commercialization in academia(L1).
- enumerate the procedure for application preparation, filing and grant of Patents(L2).
- define the terminology related to citation, citation index, h-index etc(L4).

Unit V **8L**

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. **New Developments in IPR**: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Learning Outcomes:

After the completion of this unit, the student will be able to

- explain the scope of patent rights (L1).
- describe the process for licensing and transfer of technology (L3).
- identify the sources of patent information and databases (L2).
- elaborate the administration of patent system (L5).
- describe the new developments in IPR in computer software, biological systems etc (L4).

Text Book(s):

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for Science and engineering students", Tata Mcgraw Hill India, 2013.
2. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners", 2/e, Prentice Hall of India, 2013.

References:

1. Halbert, "Resisting Intellectual Property", Taylor and Francis Limited, 2007.
2. Mayall, "Industrial Design", McGraw Hill, 1992.
3. Niebel, "Product Design", McGraw Hill, 1974.
4. Asimov, "Introduction to Design", Prentice Hall, 1962.
5. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand Publishers, 2008

Course Outcomes:

After successful completion of the course, the student will be able to

- define the meaning, sources, approaches for research problems (L2).
- explain the guidelines for carrying out effective literature review and identify research gaps (L1).
- describe effective guidelines for preparing technical reports, research publications, presentations and research proposals (L4).
- describe the codes, standards and process of obtaining intellectual property rights (L3).
- enumerate the new developments of IPR in engineering systems (L4).

19EES721: EMBEDDED C LABORATORY

L	T	P	C
0	0	4	2

Course Objectives

- To develop programs in C and assembly language for 8-bit microcontroller.
- To learn about the use of peripherals to develop embedded systems.
- To learn design of external interfacing of devices to microcontroller.
- To learn various constraints like power, speed required for an embedded system application.
- To learn the architectural differences between PIC microcontroller and 8051.

List of Experiments

1. Program in C & Assembly Language to blink LED with 1sec software delay using microcontroller8051.
2. Program to blink LED using Timers in Microcontroller8051.
3. Program to display" HelloWorld" on LCD using Microcontroller8051.
4. Program to obtain Serial Communication using Microcontroller8051.
5. Interface Keyboard & 7 Segment to using Microcontroller8051.
6. Program to blink LED using MicrocontrollerPIC16F877.
7. Program to measure Temperature using MicrocontrollerPIC16F877.
8. Program to interface Seven Segment using MicrocontrollerPIC16F877.
9. Program to test Memory using MicrocontrollerPIC16F877.
10. Program to generate PWM using MicrocontrollerPIC16F877.
11. Stepper Motor Control using MicrocontrollerPIC16F877.
12. DC Motor Control MicrocontrollerPIC16F877.

Course Outcomes

successful completion of the course, the student will be able to

- develop 8051 microcontroller programs for control of leds using Keil software and can debug(L1).
- design LCD interfacing with 8051(L2).
- write point to point data communication with 8051(L3).
- write programs for PIC microcontroller using MikroC IDE(L4).
- develop programs to control AC, DC and stepper motors(L5).

19EES723: ADVANCED DIGITAL SYSTEM DESIGN LABORATORY

L	T	P	C
0	0	4	2

Course Objectives

1. To understand Digital IC design with Verilog hardware description language
2. To construct combination circuits with Verilog.
3. To construct sequential circuits with Verilog.
4. To learn the hardware implementation details.
5. To test and verify the programs developed in Altium NB 3000 boards.

List of Experiments

1. Design and Simulation of 4-bit adder usingVerilog
2. Design of 2-to-4 decoder1u3singVerilog
3. Design of 4 bit binary to grayconverter
4. Design of Multiplexer/ Demultiplexer,comparator
5. Design of Full adder using3 modeling styles
6. Design of flip flops: SR, D, JK,T
7. Design of 4-bit binary, BCD counters (synchronous/ asynchronousreset)
8. Design of Finite StateMachine.
9. Design of UART protocol using Altiumboards
10. Basic Gates usingFPGA
11. Up- Down Counter using HDLentry
12. Implementing 16-Bit Adder Using AltiumNB3000
13. Implementing Embedded Counter UsingFPGA
14. Enabling Touch Screen On NB3000 UsingVerilog

Course Outcomes

successful completion of the course, the student will be able to

- develop Verilog models for adders, encoders, multiplexer and other combination circuits(L1).
- design flip flops and counters in Verilog(L2).
- write the programs in Verilog and simulate and synthesis the design(L3).
- write and test programs with FPGA board(L4).
- develop application using Verilog and can implement as well as debug the design(L5).

19EAC741: ENGLISH FOR RESEARCH PAPER WRITING

L	T	P	C
2	0	0	0

This course introduces the student, to the different aspects of research paper writing including planning, preparation, layout, literature review write-up etc. Specifically, the perspective and style of writing in different sections of a research paper is highlighted. Students will exposed to English language skills relevant to research paper writing.

Course Objectives:

- To write clearly, concisely and carefully by keeping the structure of the paper in mind.
- To use standard phrases in English and further improve his command over it.
- To write with no redundancy, no ambiguity and increase the readability of the paper.
- To plan and organize his paper by following a logical buildup towards a proper conclusion.
- To decide what to include in various parts of the paper.
- To write a suitable title and an abstract in order to attract the attention of the reader.
- To identify the correct style and correct tense.
- To retain the scientific value of the paper by using minimum number of words.

Unit I **5L**

Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Learning Outcomes:

After the completion of this unit, the student will be able to

- to know the expectations of various journals and referees (L2).
- to know the typical structure of a paper (L1).
- learn to put words in a sentence in the correct order (L4).
- to write short and clear sentences from the very beginning of the paper (L5).
- to increase the readability of the paper by making it easy to read and 100% clear (L3).
- learn to be concise without losing any important content (L6).
- to avoid some typical grammar mistakes made in research papers (L1).

Unit II **5L**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

Learning Outcomes:

After the completion of this unit, the student will be able to

- learn to make useful contribution worth recommending for publication (L1).
- learn good use of language to make readers notice the key findings (L3).
- learn to anticipate or predict possible objections to the claims made in the paper(L5).
- to understand what is plagiarism, and how to paraphrase other people's work (L2).
- learn to attract the right kind of readers with a suitable title(L4).
- learn to sell the abstract to potential readers by attracting their curiosity (L4).

Unit III **6L**

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Learning Outcomes:

After the completion of this unit, the student will be able to

- have a deep knowledge about everything that has been previously written on the topic and decide what is important to know in Introduction(L2).
- learn to provide the right amount of literature regarding the sequence of events leading up to the current situation in the Literature review(L1).

Unit IV **6L**

Writing Skills: skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

Learning Outcomes:

After the completion of this unit, the student will be able to

- learn to describe the materials used in experiments and/or the methods used to carry out the research (L1).
- the key skill is in reporting the results simply and clearly (L2).
- learn to structure the Discussion and satisfy the typical requirements of the referees (L1).
- learn to provide a clear and high-impact take-home message in the conclusion (L4).

Unit V **6L**

Good Paper Writing: Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

Learning Outcomes:

After the completion of this unit, the student will be able to

- learn various lists of frequently used phrases that have a general acceptance in all disciplines and use in specific sections of the paper (L1).
- learn various kinds of things one should look for when doing the final check (L2).

Text Book (s):

1. Goldbort R, Writing for Science, Yale University Press, 2006
2. Day R, How to Write and Publish a Scientific Paper, Cambridge University Press, 2006
3. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM, Highman, 1998.

References:

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Course Outcomes:

By the end of the course the students will be able to:

- frame the structure of the paper precisely (L2).
- improve his command over English by using standard phrase (L3).
- avoid repetition and mistakes in the paper and increase its readability (L3).
- organize the paper logically towards a proper conclusion (L4).
- decide on the content to be included in various parts of the paper (L5).
- identify whether to use personal or impersonal style in the paper (L5).
- express the content in a clear and concise way (L6).
- attract the attention of the reader by providing a suitable title and an appropriate abstract (L6).

19EAC742: DISASTER MANAGEMENT

L	T	P	C
2	0	0	0

This course is intended to provide fundamental understanding of different aspects of Disaster Management. It will expose the students to the concept and functions of Disaster Management and to build competencies of Disaster Management professionals and development practitioners for effective supporting environment as put by the government in legislative manner. It would also provide basic knowledge, skills pertaining to Planning, Organizing and Decision-making process for Disaster Risk Reduction.

Course Objectives:

- To provide students an exposure to disasters, their significance, types & Comprehensive understanding on the concurrence of Disasters and its management.
- To ensure that students begin to understand the relationship between vulnerability, disasters, disaster prevention, risk reduction and the basic understanding of the research methodology for risk reduction measures.
- Equipped with knowledge, concepts, and principles, skills pertaining to Planning, Organizing, Decision-making and Problem solving methods for Disaster Management.
- To develop rudimentary ability to respond to their surroundings with potential disaster response in areas where they live, with due sensitivity.

Unit I **5L**

Introduction Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Learning Outcomes

After the completion of this unit, the student will be able to

- define the meaning, list the factors and mention the significance of disaster (L3).
- distinguish between hazard and disaster (L2).
- compare manmade and natural disaster (L4).
- list the types of disaster and describe their magnitude (L1).

Unit II **5L**

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the meaning, list the factors and mention the significance of disaster (L2).
- distinguish between hazard and disaster (L1).
- compare manmade and natural disaster (L3).
- list the types of disaster and describe their magnitude (L4).

Unit III **6L**

Disaster Prone Areas in India Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the seismic zones and their characteristics (L1).
- identify the areas prone to floods and droughts (L3).
- distinguish between landslides and avalanches (L2).
- identify areas prone to cyclonic and costal hazards (L5).
- enumerate the post disaster diseases and epidemics (L3).

Unit IV **6L**

Disaster Preparedness and Management Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, media reports: governmental and Community Preparedness.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the monitoring of phenomena triggering a disaster/hazard (L1).
- evaluate the risk with the use of remote sensing and meteorological data (L5).
- list the governmental and community measures for disaster preparedness (L2).

Unit V **6L**

Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define and list the elements of disaster risk (L2).
- enumerate the measures for risk reduction (L3).
- apply the techniques of risk assessment (L1).
- identify the means of people's participation in risk assessment (L5).

Text Book(s):

1. R. Nishith, Singh A.K., Disaster Management in India: Perspectives, issues and strategies, New Royal Book Company., 2008.
2. Sahni, Pardeep, Disaster Mitigation Experiences and Reflections, Prentice Hall of India, New Delhi., 2012
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep and Deep Publication, 2007.

Course Outcomes:

At the end of the course, student will be able to

- identify management activities in pre, during and post phases of disasters (L2).
- plan disaster management activities and specify measure for risk reduction (L1).
- apply risk assessment techniques in real life disaster scenarios (L4).

19EAC743: SANSKRIT FOR TECHNICAL KNOWLEDGE

L	T	P	C
2	0	0	0

This course is intended to expose the student to the fundamentals of Sanskrit language and its technical utility in forming the core principles of many engineering branches. Students taking this course shall be able to relate the core principles of engineering branches to semantics of Sanskrit language

Course Objectives:

- to provide the knowledge of Sanskrit alphabets
- to expose the students to the basic grammar and sentence formation in past/present/future tenses
- to provide a classification of Sanskrit literature and its associated roots
- to demonstrate the relation of core engineering principles to the roots of Sanskrit literature

Unit I **9L**

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define and list the elements of disaster risk(L1).
- enumerate the measures for risk reduction(L2).
- apply the techniques of risk assessment(L4).

Unit II **9L**

Order, Introduction of roots, Technical information about Sanskrit Literature.

Learning Outcomes

After the completion of this unit, the student will be able to

- classify the different branches of Sanskrit literature(L1).
- describe the order and roots of Sanskrit literature(L2).
- relate the applicability of Sanskrit literature to technical principles(L5).

Unit III **9L**

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Learning Outcomes

After the completion of this unit, the student will be able to

- relate the technical concepts of engineering to principles of electrical technology(L1).
- relate the technical concepts of engineering to principles of mechanical engineering(L4).
- apply the use of Sanskrit knowledge to describe the mathematical principles(L3).

Text Book(s):

1. Dr.Vishwas, Abhyaspustakam, Samskrita Bharti Publication, New Delhi, 2005.
2. Vempati Kutumb Shastri, Teach Yourself Sanskrit, Prathama Deeksha, Rashtriya Sanskrit Sansthanam, New Delhi Publication, 2003.
3. Suresh Soni, India's Glorious Scientific Tradition, Ocean books, New Delhi, 2011.

Course Outcomes:

After successful completion of the course, the student will be able to

- get a working knowledge in illustrious Sanskrit, the scientific language in the world (L2).
- get a Learning of Sanskrit to improve brain functioning (L1).
- develop the logic in mathematics, science & other subjects with principles of Sanskrit(L4).
- explore the huge knowledge from ancient literature with the help of Sanskrit (L5).

19EAC744: VALUE EDUCATION

L	T	P	C
2	0	0	0

This course is intended to expose the student to the need for human values and methods to cultivate them for leading an ethical life with good moral conduct. Students taking this course will be able to experience a change in personal and professional behavior with these ethical principles guiding him throughout life

Course Objectives:

- To expose the student to need for values, ethics, self-development and standards
- To make the student understand the meaning of different values including duty, devotion, self-reliance etc.
- To imbibe the different behavioral competencies in students for leading an ethical and happy life
- To expose the student to different characteristic attributes and competencies for leading a successful, ethical and happy profession life.

Unit I **7L**

Values and self-development –social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the social values and individual attitudes for self-development (L2).
- describe the Indian vision of humanism (L1).
- distinguish between moral and non-moral acts (L3).
- list the standards and value principles for moral conduct (L5).

Unit II **7L**

Importance of cultivation of values. Sense of duty. Devotion, self-reliance. Confidence, concentration. Truthfulness, cleanliness. Honesty, humanity. Power of faith, national unity. Patriotism, love for nature, discipline.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the importance of cultivating values (L1).
- list the different traits of self-developed individual (L3).
- explain the need for loving nature/country/humanity (L2).

Unit III **7L**

Personality and Behaviour Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the benefits of positivie thinking, integrity and discipline (L2).
- list the different methods for avoiding fault finding, anger (L4).
- explain the methods to overcome suffering, religious intolerance, self-destructive habits (L3).

Unit IV **7L**

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind,

Self-control. Honesty, Studying effectively.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the science of reincarnation (L2).
- explain the relation between self-management and good health (L1).
- elaborate the role of different religions in reaching the common goal (L4).
- list the different techniques for mind-control to improve personality and studies (L3).

Text Book(s):

1. Chakroborty S.K., "Values and ethics for organizations: Theory and Practice", Oxford University Press, 1998.

Course Outcomes:

After successful completion of the course, the student will be able to

- appreciate the need for human values and methods for self development (L2).
- elaborate the different traits and benefits of a self-developed individual (L1).
- list the different attributes of self-developed individual (L4).
- elaborate the role and scope of books/faith/health/religions in character building and competence development (L3).

19EAC745: CONSTITUTION OF INDIA

L	T	P	C
2	0	0	0

This course is intended to expose the student to the philosophy of Indian constitution.
Students will be able to understand their fundamental rights/duties and governance structure. Students also appreciate the role of election commission in establishing a democratic society.

Course Objectives:

- To familiarize the student about the need for a constitution
- To make the student understand the role of constitution in a democratic society
- To acquaint the student with key constitutional features and fundamental rights of a citizen
- To impart the organs of governance and local administration hierarchy and their responsibilities
- To familiarize the student with the role, responsibilities and administration hierarchy of election commission

Unit I **5L**

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working). **Philosophy of the Indian Constitution**: Preamble, Salient Features

Learning Outcomes:
After the completion of this unit, the student will be able to

- list the outline of drafting committee and their roles in the making of Indian constitution (L1)
- describe the need and role of a constitution in a democratic society (L1)
- elaborate the salient features of Indian constitution (L2)

Unit II **5L**

Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Learning Outcomes:
After the completion of this unit, the student will be able to

- list the fundamental rights of a citizen (L2)
- explain the intricacies in the different rights (L3)
- elaborate the fundamental duties of a citizen (L3)
- describe the principles of state policy (L4)

Unit III **6L**

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions

Learning Outcomes:
After the completion of this unit, the student will be able to

- present the hierarchy of governance (L3)
- list the role/responsibilities/powers of different organs of governance (L4)
- elaborate the guidelines for appointment/transfer of judges (L5)

Unit IV **6L**

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Panchayat raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root

democracy.

Learning Outcomes:
After the completion of this unit, the student will be able to

- describe the administrative organizational hierarchy of municipalities and panchayats(L4)
- appreciate the role/responsibilities/powers of mayor, CEO, elected officials (L5)
- appreciate the importance of grass root democracy (l5)

Unit V **6L**

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Learning Outcomes:
After the completion of this unit, the student will be able to

- describe the administrative hierarchy of election commission (L5)
- elaborate the roles/responsibilities/powers of election commissioners at different levels of hierarchy (L5)
- outline the welfare activities of SC/ST/OBC/Women by different bodies (L4 & L5)

Text Book(s):

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. S. N. Busi, Dr. B. R. Ambedkar, Framing of Indian Constitution, 1/e, 2015.
3. M. P. Jain, Indian Constitution Law, 7/e, Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes:

After successful completion of the course, the student will be able to

- describe the philosophy and salient features of Indian constitution (L1)
- list the constitutional rights and duties of a citizen (L3)
- elaborate the central and local administrative hierarchy and their roles (L2)
- describe the roles/responsibilities/powers of different governing and administrative bodies (L4)
- explain the structure/functioning and power of election commission (L5)

19EAC746: PEDAGOGY STUDIES

L	T	P	C
2	0	0	0

This course is aimed to familiarizing the student with pedagogical principles, practices and methodologies. This course is intended for students interested in pursuing a career in teaching and research.

Course Objectives:

- To familiarize the student about the need for pedagogy studies, background and conceptual framework
- To expose the student to pedagogical practices in formal/informal classrooms
- To acquaint the student with type of curriculum and guidance materials for effective pedagogy
- To familiarize the student with classroom practices and curriculum assessment procedures
- To make the student understand the effect of undertaking research on teaching quality

Unit I **5L**

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the aim and rationale behind teacher education (L2).
- classify the different theories of learning (L1).
- elaborate the need and role of curriculum, teacher education (L3).

Unit II **5L**

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the different pedagogical practices used by teachers in formal and informal classrooms(L2).
- explain the pedagogical practices employed in developing countries (L1).
- enumerate the duties of faculty in terms of teaching, research, consultancy, administration (L4).

Unit III **6L**

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the measures for effective pedagogy (L1).
- identify the different documentation required to formalize curriculum implementation and quality assessment (L3).

- describe the teachers attitudes and beliefs in pedagogic strategies (L4).

Unit IV **6L**

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the organizational hierarchy in a school administration system (L3).
- list the different barriers to learning (L1).
- enumerate the methods to overcome limited resources and handle large class sizes (L4).
- describe the follow-up support and peer-support in classroom practices (L2).

Unit V **6L**

Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Learning Outcomes:

After the completion of this unit, the student will be able to

- explain the need for and role of research in teaching profession (L1).
- list the different research activities to be taken up by teachers (L2).
- describe the impact of research on teaching quality and learning process (L4).

Text Book(s):

1. Ackers J, Hardman F, Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261, 2001
2. Agrawal M, Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379, 2004.
3. Akyeampong K, Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID., 2003.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J, Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282., 2013.
5. Alexander RJ, Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell., 2001.
6. Chavan M, Read India: A mass scale, rapid, ‘Learning to Read’ campaign., 2003.

Course Outcomes:

After successful completion of the course, the student will be able to

- describe the theories of learning and conceptual framework of pedagogy (L2).
- explain the pedagogical practices used by teachers in formal and informal classrooms (L1).
- visualize the administrative hierarchy of schools and colleges and define the role (L4).
- appreciate the need for research and define the future direction of teaching career (L3).
- describe the impact of curriculum and assessment on the teaching learning process of a student (L5).

19EAC747: STRESS MANAGEMENT BY YOGA

L	T	P	C
2	0	0	0

This course is aimed to familiarize the student with basic principles of yoga and different physical/mental practices for managing mind and body. This course helps the student in managing stress during education, home and workplace. Further, principles learnt in this course help in building overall personality for a stress-free, happy and independent life.

Course Objectives:

- To familiarize the student about eight parts of yoga and their significance
- To expose the student to the importance and meaning of Yam and Niyam
- To make the student understand the meaning and importance of yogic principles including Ahimsa, Satya, Astheya etc
- To introduce the different yogic poses with a knowledge of their benefits for mind and body
- To familiarize the effect of different types of breathing techniques in concept and in activity

Unit I **9L**

Definitions of Eight parts of yoga (Ashtanga).

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the eight parts of yoga(L2).
- describe the effects of different parts of yoga on mind and body(L1).
- elaborate the importance of yoga in stress management and personality development(L3).

Unit II **9L**

Yam and Niyam.
Do`s and Don't's in life.

i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan.

Learning Outcomes:

After the completion of this unit, the student will be able to

- elaborate the importance of Yam and Niyam (L2).
- describe the meaning and significance of Ahinsa, satya, astheya etc (L1).
- explain the need for shaucha, santosh, tapa, swadhyay in leading a healthy and fruitful life (L3).

Unit III **9L**

Asan and Pranayam

i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its Effects-Types of pranayam.

Learning Outcomes:

After the completion of this unit, the student will be able to

- demonstrate the different physical asanas and explain their physical and phychological effects(L1).
- demonstrate the different breathing techniques and describe their physical and mental effects (L3).
- distinguish between different types of pranayamam(L4).

Text Books

1. Janardan, Yogic Asanas for Group Tarining-Part-I, Swami Yogabhyasi Mandal, Nagpur
2. Swami Vivekananda, "Rajayoga or conquering the Internal Nature", Advaita Ashrama, Kolkata

Course Outcomes:

After successful completion of the course, the student will be able to

- describe the eight parts of yoga and their significance (L1).
- explain the the importance and meaning of Yam and Niyam (L3).
- define the meaning and importance of yogic principles including Ahimsa, Satya, Astheya etc (L2).
- demonstrate the different yogic poses and explain their benefits for mind and body (L4).
- demonstrate the different types of breathing techniques and explain their physical and mental benefits (L5).

19EAC748: PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

L	T	P	C
2	0	0	0

This course is aimed to familiarize the student with life enlightenment skills for personality development. This course helps the student in building his holistic personality through human values, ethics and spiritual attributes.

Course Objectives:

- To familiarize the student to good personality traits through moral stories
- To make the student understand the goal of human life and importance of good personality in reaching the goal
- To expose the student to the study of Shrimad-Bhagwad-Geeta for developing his/her personality and achieve the highest goal in life
- To familiarize the student to leadership skills for driving nation and mankind to peace and prosperity
- To expose the role of Neetishatakam for developing versatile personality of students.

Unit I **9L**

Neetisatakam-Holistic development of personality
Verses- 19,20,21,22 (wisdom)
Verses- 29,31,32 (pride & heroism)
Verses- 26,28,63,65 (virtue)
Verses- 52,53,59 (dont's)
Verses- 71,73,75,78 (do's).

Learning Outcomes:
After the completion of this unit, the student will be able to

- describe the moral stories illustrating the traits of good personality (L1)
- define the meaning and importance of wisdom, pride, heroism, virtue etc (L2)
- identify do and donts in life from the foundations of human morals/ethics (L2)

Unit II **9L**

Approach to day to day work and duties.
Shrimad BhagwadGeeta: Chapter 2-Verses 41, 47,48,
Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
Chapter 18-Verses 45, 46, 48.

Learning Outcomes:
After the completion of this unit, the student will be able to

- describe the characteristics and principles of bhakti yogam, jnana yogam and karma yogam (L3)
- identify the use of different yogic characteristics in different activities of daily life/duties (L4)
- apply the use of yogic principles for leading a stress-free, happy and fruitful life with good developed personality (L4)

Unit III **9L**

Statements of basic knowledge.
Shrimad BhagwadGeeta: Chapter2-Verses 56, 62, 68
Chapter 12 -Verses 13, 14, 15, 16,17, 18
Personality of Role model. Shrimad BhagwadGeeta:
Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
Chapter 4-Verses 18, 38,39
Chapter18 – Verses 37,38,63

Learning Outcomes:

After the completion of this unit, the student will be able to

1. list the characteristics of role model proposed by verses of bhagavad gita (L3)
2. explain the methods for obtaining life enlightenment through the practice of four yoga appropriately (L4)
3. describe the characteristics of karma yogi/jnana yogi for developing leadership personality (L5)

Text Book(s):

1. Swami Swarupananda, "Srimad Bhagavad Gita", Advaita Ashram (Publication Department), Kolkata
2. P. Gopinath, Bhartrihari's Three Satakam (Niti-Sringar-vairagya), Rashtriya Sanskrit Sansthanam, New Delhi.

Course Outcomes:

After successful completion of the course, the student will be able to

- List the different parables of neethisathakam and identify their morals (L1)
- enumerate the different traits of human personality for life enlightenment (L2)
- describe the leadership attributes for driving nation and mankind to peace and prosperity (L3)
- explain the applicability of different types of yoga to day-to-day work and duties resulting in responsible personality (L4)

19EAC750: DEVELOPING SOFT SKILLS AND PERSONALITY

L	T	P	C
2	0	0	0

Soft skills comprise pleasant and appealing personality traits as self-confidence, positive attitude, emotional intelligence, social grace, flexibility, friendliness and effective communication skills. The course aims to cause a basic awareness within the students about the significance of soft skills in professional and inter-personal communications and facilitate an all-round development of personality.

Course Objectives

- to familiarize the student to the criteria for self assessment and significance of self-discipline
- to expose the student to attitudes, mindsets, values and beliefs
- to acquaint the student to plan career and goals through constructive thinking
- to enable the student to overcome barriers for active listening and persuasive speaking
- to familiarize the skill of conducting meetings, writing minutes and involving in active group discussions

Unit I **(8L)**

Self-Assessment; Identifying Strength & Limitations; Habits, Will-Power and Drives; Developing Self-Esteem and Building Self-Confidence, Significance of Self-Discipline

Learning Outcomes

After the completion of this unit, the student will be able to

- identify strengths & limitations through self-assessment(L3)
- list the attributes of personalities will good will-power and self-drives(L1)
- describe the reasons for building self-esteem and self-confidence(L2)
- explain the significance of self discipline(L2)

Unit II **(8L)**

Understanding Perceptions, Attitudes, and Personality Types: Mind-Set: Growth and Fixed;
Values and Beliefs

Learning Outcomes

After the completion of this unit, the student will be able to

- define the characteristics of different perceptions, attitudes and personality types(L1)
- distinguish between fixed and growing mindsets(L3)
- define the importance and meaning of values and beliefs(L2)

Unit III **(8L)**

Motivation and Achieving Excellence; Self-Actualisation Need; Goal Setting, Life and Career Planning; Constructive Thinking

Learning Outcomes

After the completion of this unit, the student will be able to

- describe the need for having high motivation and achieving excellence(L2)
- define the need for self-actualization(L1)
- plan the life and career goals based on self assessment(L4)
- explain the attributes of constructive thinking(L2)

Unit IV **(8L)**

Communicating Clearly: Understanding and Overcoming barriers; Active Listening; Persuasive Speaking and Presentation Skills.

Learning Outcomes

After the completion of this unit, the student will be able to

- self-assess the barriers for communicating clearly (L4)

- list the attributes of active listening(L1)
- describe the minimal aspects of effective presentation(L2)
- organize ideas resulting a persuasive talk(L3)

Unit V **(8L)**

Conducting Meetings, Writing Minutes, Sending Memos and Notices; Netiquette: Effective E-mail Communication; Telephone Etiquette; Body Language in Group Discussion and Interview.

Learning Outcomes

After the completion of this unit, the student will be able to

- describe the format and structure of writing meeting minutes(L2)
- identify the essential components of memos and notices(L3)
- explain the principles of effective email communication(L2)
- list the basic etiquette of telephone conversation(L1)
- describe the effective body traits during group discussion and interviews(L2)

Text Books

1. Dorch, Patricia. What Are Soft Skills? New York: Execu Dress Publisher, 2013.
2. Kamin, Maxine. Soft Skills Revolution: A Guide for Connecting with Compassion for Trainers, Teams, and Leaders. Washington, DC: Pfeiffer & Company, 2013.
3. Klaus, Peggy, Jane Rohman& Molly Hamaker. The Hard Truth about Soft Skills. London: HarperCollins E-books, 2007.
4. Petes S. J., Francis. Soft Skills and Professional Communication. New Delhi: Tata McGraw-Hill Education, 2011.
5. Stein, Steven J. & Howard E. Book. The EQ Edge: Emotional Intelligence and Your Success. Canada: Wiley & Sons, 2006.

Course Outcomes

After successful completion of the course, the student will be able to

- carry out self assessment and describe the significance of self-discipline(L4)
- define, classify and compare attitudes, mindsets, values and beliefs(L3)
- plan career and goals through constructive thinking and personal assessment(L4)
- overcome barriers for active listening and persuasive speaking (L5)
- conduct meetings, write minutes and involve in active group discussions(L3)

19EES702: ADVANCED MICROCONTROLLERS

L T P C
3 0 0 3

This course introduces the students, to advanced 32bit microcontroller and applications. The first two units cover the architecture of AVR microcontroller and its interfacing with peripherals. The next two units cover various advanced ARM microcontroller architecture and application development with OS. The last unit covers design of applications with ARM

Course objectives:

- To learn about the AVR microcontroller fundamentals and importance.
- To acquaint with the peripheral programming of AVR microcontrollers.
- To familiar with 32bit ARM microcontrollers architecture and its advantages.
- To learn about the signal processing with ARM microcontrollers and RTO's.
- To develop applications with wired and wireless devices.

Unit I: AVR Microcontroller Architecture (8L)

Architecture, memory organization, addressing modes, programming techniques, assembly language & C programming, development tools, cross compilers, hardware design issues.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the architecture of AVR RISC microcontroller and pin diagram (L2).
- select the development tools and IDE for AVR microcontroller(L1).
- what are the addressing modes used in AVR microcontroller(L1).

Unit II : Peripheral of AVR Microcontroller (8L)

I/O memory, EEPROM, I/O ports, SRAM, timer, UART, interrupt structure, serial communication with PC, ADC/DAC interfacing.

Learning Outcomes:

After completion of this unit the student will be able to

- explain peripherals of AVR microcontroller(L2).
- how the serial bus communication done in AVR microcontroller(L1).
- construct the interfacing of ADC to AVR (L3).

Unit III: ARM Architecture and Programming (9L)

Arson RISC machine, architectural inheritance, core & architectures, registers, pipeline, interrupts, ARM organization, Differences between ARM and thumb instruction set, the ARM programmer's model, ARM development tools, ARM assembly language programming and C compiler programming.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the architecture of ARM microcontroller and 3 stage pipelining (L2).
- interpret the ARM programmers model and modes (L2).
- demonstrate the instruction set and tool chain of ARM processors(L2).

Unit IV: ARM Application Development (9L)

Introduction to DSP on ARM, FIR filter, IIR filter, exception handling, interrupts, interrupt handling schemes, standalone, embedded operating systems, fundamental components, and example simple little operating system.

Learning Outcomes:

After completion of this unit the student will be able to

- Choose standalone or embedded OS development with ARM microcontroller (L3).
- Outline the ARM interrupts and exceptions (L2).
- Solve DSP on ARM processors to implement DSP filters such as FIR and IIR(L3).

Unit V: Design with ARM Microcontrollers (8L)

Integrated development environment, STDIO libraries, user peripheral devices, application of ARM processor: wireless sensor networks, robotics.

Learning Outcomes:

After completion of this unit the student will be able to

- show the use of IDE and use of STDIO libraries with ARM microcontroller (L2).
- construct Wireless sensor networks with ARM (L6).
- build line following robot with ARM(L6).

Text Books:

1. Steve Furber, ARM system on chip architecture, 2/e, Addision Wesley,2001.
2. Dananjay V. Gadre, Programming and Customizing the AVR microcontroller, McGraw Hill,2001.

References

1 AndrewN.Sloss,Domini$_2$c$_7$Symes,ChrisWright,JohnRayfield,ARMSystemDeveloper'sGuide Designing and Optimizing System Software,3/e, Elsevier, 2007.

2 Trevor Martin, the Insider's Guide to the Philips ARM7-Based Microcontrollers,anEngineer's Introduction to the LPC2100 Series,2005.

3 ARM Architecture ReferenceManual.

Course Outcomes:

successful completion of the course, the student will be able to explain

- The basic concepts of AVR microcontroller architecture and addressing modes (L1).
- The instruction set and peripheral programming of AVR microcontrollers (L2).
- The architecture of ARM microcontrollers (L3).
- The basic concepts in developing the applications with and without OS (L4).
- The concepts in wireless sensor networks with ARM and to develop robotic applications (L5).

19EES742: DIGITAL VLSI DESIGN

L T P C
3 0 0 3

This course introduces the students, to digital VLSI design process and implementation details. The first two units cover the IC technology and VLSI designflow. The next two units design gates using MOS switches and sub system design. The last unit covers implementation of the design on FPGA.

Course objectives:

1. To understand MOS, PMOS, NMOS, CMOS & BICMOS technologies
2. To understand various processes in VLSI Circuit Design
3. To understand basic VLSI circuit concepts and gate level design
4. To study subsystem design in VLSI circuit
5. To understand IC Design, VHDL synthesis and IC testing

UnitI **9L**

Introduction: Introduction to IC technology: MOS, PMOS, NMOS, CMOS& BICMOS technologies-oxidation, lithography, diffusion, ion implantation, metallization, encapsulation, probe testing, integrated resistors and capacitors. Basic Electrical Properties: Basic electrical properties of MOS and BICMOS circuits, ids-vs. relationships, MOS transistor threshold voltage, gm, gds, figure of merit do, pass transistor, NMOS inverter, various pull ups, CMOS inverter analysis and design, BI-CMOS inverters.

Learning Outcomes:

After completion of this unit the student will be able to

- Explain the IC design flow and technology to implement(L1)
- Demonstrate the steps of design of inverter with NMOS and PMOS (L2)
- Summarize NMOS inverter, CMOS inverter and BI-CMOS inverters (L2)

UnitII **9L**

VLSI Circuit Design Processes: VLSI design flow, MOS layers, stick diagrams, layout design rules, 2 μm CMOS design rules for wires, contacts and transistors layout diagrams for NMOS and CMOS inverters and gates, scaling of MOS circuits, limitations of scaling.

Learning Outcomes:

After completion of this unit the student will be able to

- Outline VLSI design flow(L2)
- Demonstrate the stick diagrams and rules (L2)
- Relate scaling and limitations (L2)

UnitIII **8L**

Gate Level Design: Logic gates and other complex gates, switch logic, alternate gate circuits, basic circuit concepts, sheet resistance RS and its concept to MOS, area capacitance Unit s, calculations - t - delays, driving large capacitive loads, wiring capacitances, fan-in and fan-out, choice of layers.

Learning Outcomes:

After completion of this unit the student will be able to

- Construct gates with MOS switches (L3).
- Classify driving loads (L2).

- Illustrate fan-in and fan-out characteristics (L2).

UnitIV **8L**

Subsystem Design: Subsystem design, shifters, adders, single-bit adder, n-bit parallel adder, ALUS, multipliers, parity generators, comparators, zero/one detectors, counters- asynchronous and synchronous, high density memory elements.

Learning Outcomes:

After completion of this unit the student will be able to

- What is a subsystem and subsystem design(L1).
- Build combinational circuits (L3).
- Build sequential circuits (L3).

UnitV **8L**

Semiconductor Integrated Circuit Design: PLAS, FPGAS, CPLDS, standard cells, programmable array logic, design approach. VHDL Synthesis: VHDL synthesis, circuit design flow, circuit synthesis, simulation, layout, design capture tools, design verification tools, test principles. CMOS Testing: need for testing, test principles, design strategies for test, chip level test techniques, system-level test techniques, and layout design for improved testability.

Learning Outcomes

After completion of this unit the student will be able to

- Plan to implement the design in PLAS, FPGAS, CPLDS (L3).
- Demonstrate VHDL synthesis (L2).
- Explain CMOS testing techniques (L2).

Text Books:

1 Kamran Eshraghian, Eshraghian Dougles and A.Pucknell, Essentials of VLSI circuits andsystems, Prentice Hall ofIndia, 2005.
2 Neil H. Weste, Eshraghian, Principles of CMOS VLSI Design, Pearson Education,1999.

References

1. John P. Uyemura, Chip Design for Submicron VLSI: CMOS Layout and Simulation, Thomson Learning,2006.
2. John. P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley and Sons,2003.
3. John M. Rabaey, Digital Integrated Circuits, PHI, EEE,1997.
4. Wayne Wolf, Modern VLSI Design, 3/e, Pearson Education,1997.

Course Outcomes

successful completion of the course, the student will be able to

- describe the various technologies used for VLSI design and their features (L1).
- understand VLSI design flow, stick diagrams and layout diagrams (L2).
- describe Logic gates, alternate gate circuits and calculation of delays (L3).
- design various arithmetic and logic circuits in VLSI (L4).
- understand programmable devices, simulation and testing of VLSI devices (L5).

19EES744: FUNDAMENTALS OF CRYPTOGRAPHY AND NETWORK SECURITY

L	T	P	C
3	0	0	3

This course introduces the students, to cryptography techniques and network security. The first two units cover encryption techniques and cipher design algorithms. The next two units cover the importance of public key encryption and digital signature standards to avoid security attacks. The last unit covers firewalls and web security.

Course objectives:

1. To understand encryption techniques and cryptanalysis
2. To understand the concept of cipher and its design principles and algorithms
3. To understand the public encryption and key management
4. To study security and authentication algorithms
5. To understand E-mail security and web security

UnitI **9L**

Introduction: Security attacks, security services, security mechanisms, model for network security, classical encryption techniques: symmetric cipher model, substitution techniques, transposition techniques, steganography, block ciphers and the data encryption standard: block cipher principles, data encryption standard, strength of DES, differential and linear cryptanalysis.

Learning Outcomes

After completion of this unit the student will be able to

- explain security attacks and encryption techniques (L2).
- demonstrate block ciphers and the data encryption standard (L2).
- choose differential or linear cryptanalysis. (L1).

UnitII **9L**

Block cipher design principles, block cipher mode operation, and triple DES, AES algorithm, stream ciphers, RC4. Introduction to number theory, modular arithmetic, Euclidean algorithm, prime numbers, Fermats and Eulers theorem, testing for primality, Chinese remainder theorem, discretelogarithms.

Learning Outcomes:

After completion of this unit the student will be able to

- explain Block cipher design principles, operations and DES, AESalgorithms (L2).
- summarize number theory used in cryptography (L2).
- illustrate Euclidean algorithm (L2).

UnitIII **8L**

Public Key Cryptography: Principles of public key cryptosystems, RSA algorithm, key management, key management, Diffie-Hellman key exchange. Message authentication and hash functions: authentication requirements and authentication functions, MAC, hash functions.

Learning Outcomes:

After completion of this unit the student will be able to

- show the importance of public key cryptosystems (L2).

- apply RSA algorithm (L3).
- illustrate key management and hash functions (L2).

UnitIV **8L**

Hash Algorithms: Secure hash algorithm, whirlpool, MAC, CMAC, digital signatures & Authentication protocols: digital signatures, standard, authentication Applications: kerberos, X.509 authenticationservice.

Learning Outcomes:

After completion of this unit the student will be able to

- summarize secure hash algorithms (L2).
- demonstrate authentication protocols used in cryptography (L2).
- illustrate kerberos, X.509 authentication service. (L2).

UnitV **8L**

Electronic mail security, IP security, web security, firewalls.

Learning Outcomes:

After completion of this unit the student will be able to

- explain about the Electronic mail security (L2).
- demonstrate IP security (L2).
- classify web security and firewalls. (L2).

Text Book

1. William Stallings, Cryptography and Network Security - Principles and Practices, 4/e, Pearson Education, 2006.

References

1. Charlie Kaufman, Radia Perlman, Mike Speciner, Network Security: Private Communication ina Public World, 2/e, Prentice29Hall.
2. Eric Maiwald, Fundamentals of NetworkSecurity, TATAMcGraw-Hill,2003.
3. Contemporary Cryptography. Birkhauser. Springer International, Yes DeePublications.

Course Outcomes

successful completion of the course, the student will be able to

- understand about security attacks, the block cipher and its analysis (L1).
- know about different cryptographic algorithms and related number theory (L2).
- understand public encryption and use of hash functions (L3).
- understand about digital signature standards (L4).
- know about the network security (L5).

	L	T	P	C
19EES746: ROBOTICS ANDCONTROL	**3**	**0**	**0**	**3**

This course introduces the students, to types of robotics and its applications. The first two units types of robotics and the sensors used and selection of the sensors. The next two units cover the actuators, grippers used in various robotic applications. The last unit covers implementation of control system algorithms.

Course objectives:

1. To learn about basics of robots.
2. To describe the working of various drives and sensors.
3. To describe the concepts of manipulators and related actuator modes.
4. To know about different sensors and their applications.
5. To learn various controller methods for control of manipulators.

UnitI **8L**

Basic Concepts: Definition and origin of robotics, different types of robotics, various generations of robots, degrees of freedom, Asimov's laws of robotics, anatomy of robot, applications of robots.

Learning Outcomes:

After completion of this unit the student will be able to

- match different types of robots based on the application (L1).
- demonstrate anatomy of robot (L2).
- outline degrees of freedom (L2).

UnitII **8L**

Sources and Sensors: Hydraulic, pneumatic and electric drives, determination of hp of motor and gearing ratio, variable speed arrangements, path determination, micro machines in robotics, machine vision, ranging, laser, acoustic, magnetic, fiber optic and tactile sensors.

Learning Outcomes:

After completion of this unit the student will be able to

- examine different sensors used in robotics based on the application (L4).
- show the drives used in robots (L2).
- outline robot vision (L2).

UnitIII **9L**

Manipulators, Actuators and Grippers: Construction of manipulators, manipulator dynamics and force control, types of control modes, electronic and pneumatic manipulator control circuits, end effectors, various types of grippers.

Learning Outcomes:

After completion of this unit the student will be able to

- spell construction of manipulators (L1).
- demonstrate various types of grippers (L2).
- illustrate the dynamics in gripper design (L2).

UnitIV **9L**

Robotic Sensors Applications: Sensing, sensors in robotics, kinds of sensors used in robotics, robotic vision, robotic vision systems image acquisition, image representation, image processing, industrial robotic vision, industrial applications of vision controlled robotic systems applications, process of imaging, architecture of applications, material handling, process.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate image acquisition and its processing (L2).
- explain the industrial applications of vision controlled robotic systems applications (L2).
- how the robots used in material handling, process (L1).

UnitV **8L**

Control of Manipulators: PID control computed, torque technique, near minimum time control, variable structure control, non-linear decoupled feedback control, resolved motion control and adaptive control.

Learning Outcomes:

After completion of this unit the student will be able to

- apply PID control algorithm (L3).
- illustrate noon linear feedback control (L3).
- explain adoptive control (L2).

TextBooks:

1. Saeed B. Niku, Introduction to Robotics Analysis, Systems, Applications, Pearson Education,2001.
2. Mikell P. Groover, Industrial Robots- Technology Programming and Applications, McGraw Hill,1980.

References

1. Yoran Koren, Robotics for Engineers, McGrawHill,1980.
2. Craig,IntroductiontoRoboticsMechanicsand Control,2/e,PearsonEducation, 2004.
3. Satya Ranjan Deb, Robotics Technology and Flexible Automation, TMH,2001.
4. Asada and Slotine, Robot Analysis and Control, John Wiley,1986.

Course Outcomes

successful completion of the course, the student will be able to

- understand about anatomy of robots, history behind the robots (L1).
- know about different drive systems and also about various sensors (L2).
- select suitable manipulator dynamics and related grippers (L3).
- understand about the sensors used in industrial applications (L4).
- design a process control system using advanced controllers (L5).

19EES748: NEURAL NETWORKS AND FUZZY SYSTEMS

L	T	P	C
3	0	0	3

This course introduces the students, to intelligent non conventional control algorithms with neural networks and fuzzy logic. The first two units what is neural model and layers in neural network. The next unit covers how to train the neuron with Unsupervised Learning. The last two units cover the concepts fuzzy logic and hybrid Neuro fuzzy control system.

Course objectives:

1. To know the Difference between artificial neuron and human brain.
2. To solve the logical function with artificial neural network.
3. To study the supervised and unsupervised learning methods.
4. To know the difference between classical sets and fuzzy sets.
5. To understand the classical and fuzzy logic decision making.

UnitI **8L**

Introduction to Artificial Neural Networks: Artificial neural networks and their biological motivation, terminology, models of neuron, topology, characteristics of artificial neural networks, types of activation functions. learning laws: learning methods, error correction learning, hebbian learning, perceptron, XOR problem, perception learning rule convergence theorem, adaline.

Learning Outcomes

After completion of this unit the student will be able to

- classify perceptron and neuron (L2).
- explain the XOR problem in neural network (L2).
- illustrate the characteristics of a neuron (L1).

UnitII **8L**

Feed forward networks: Multilayer perceptron, back propagation learning algorithm, universal function approximation, Associative memory: auto association, hetero association, recall and cross talk. Recurrent neural networks: linear auto associator, Bi-directional associative memory, Hopfield neural network, Traveling SalesmanProblem.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate the back propagation learning algorithm (L2).
- summarize the Recurrent neural networks (L2).
- analyze the Traveling Salesman Problem with neural network (L1).

UnitIII **8L**

Unsupervised Learning: Competitive learning neural networks, Max net, Mexican hat, hamming net. Self-organizing networks: Kohonen Self organizing feature map, counter propagation, learning vector quantization adaptive resonance theory. Applications of neural networks in image processing signal processing, modeling and control.

Learning Outcomes:

After completion of this unit the student will be able to

- explain how to train the neuron (L2).

- demonstrate self-organizing networks (L2).
- identify the applications of neural networks in image processing signal processing, modeling and control (L3).

UnitIV **9L**

Fuzzy Sets and Fuzzy Relations: Introduction, classical sets and fuzzy sets, classical relations and fuzzy relations, membership functions, fuzzy to crisp conversion, fuzzy arithmetic, numbers, vectors, and extension principle.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate the what is a fuzzy logic and its membership functions (L2).
- classify crisp vs fuzzy logic (L4).
- apply fuzzy operations on fuzzy sets (L3).

UnitV **9L**

Fuzzy Decision Making: Classical logic and fuzzy logic, fuzzy rule based systems, fuzzy nonlinear simulation, fuzzy decision making, fuzzy control systems, fuzzy optimization, one-dimensional optimization.
Neuro Fuzzy: Mathematical formulation of adaptive neuro, fuzzy inference systems.

Learning Outcomes:

After completion of this unit the student will be able to

- analyze fuzzy rule based systems (L4).
- illustrate fuzzy decision making with the rule base (L2).
- explain the need for hybrid Neuro fuzzy systems (L2).

Text Books:

1. Laurence Fausett, Fundamentals of Neural Networks-Architectures, algorithms andapplications, 3/e, Pearson Education Inc,2008.

References

1. J.S.R. Jang, C.T. Sun, E. Mizutani, Neuro Fuzzy and Soft Computing - A Computational Approach to Learning and Machine Intelligence, Pearson Education,2008
2. S.Haykin, Neural Networks- A Comprehensive Foundation, 2/e, Pearson Education,2004.
3. Jacek M. Zurada, Introduction to Artificial Neural Systems, Jaico Publishing House,2001.
4. Timothy J. Ross, Fuzzy Logic with Engineering Applications, 3/e, John Wiley and Sons,2010.

Course Outcomes:

successful completion of the course, the student will be able to

- obtain the fundamentals, Characteristics, learning laws and types of neural networks (L1).
- have adequate knowledge about feedback neural networks (L2).
- apply the neural networks in image, signal processing modelling and control (L3).
- write the differences of classical, fuzzy sets and relations (L4).
- application of fuzzy logic optimization in the real time applications (L5).

19EES750: DIGITAL SYSTEMS TESTING AND TESTABILITY

L	T	P	C
3	0	0	3

This course introduces the students, to testing and verification in VLSI design process. The first unit covers various fault models and their simulation. The next three units covers various ATPG methods to detect faults in combinational and sequential circuits. The last covers BIST schemes.

Course Objectives:

1. To provide detection techniques for faults occurring in digital systems
2. To explore glossary of fault models to simplifying the detection
3. To generate test vectors to detect and diagnose the faults using various algorithms
4. To provide knowledge about designing of Testable Combinational and Sequential circuits/Memory systems
5. To recognize the BIST techniques for improving testability

UnitI **10L**

Introduction: Introduction, testing philosophy, role of testing, digital and analog VLSI testing. VLSI Testing Process and Test Equipment: How to test chips. Test Economics and Product Quality: Test economics, yield. Fault Modeling: defects, errors and functional versus structural testing, levels of fault models, glossary of fault models, single stuck-at fault. Logic and Fault Simulation: Simulation for design verification, simulation for test evaluation, modeling circuits for simulation, algorithms for true- value simulation, algorithms for fault simulation, statistical methods for fault simulation.

Learning Outcomes:

After completion of this unit the student will be able to

- apply the concepts in testing which can help design a better yield in IC design (L1).
- use the appropriate test algorithm methods for achieving certain fault coverage specifications in design (L2).
- differentiate between defect, fault and error (L1).

UnitII **9L**

Combinational Circuit Test Generation: Algorithms and representations, redundancy identification (RID), testing as a global problem, definitions, significant combinational ATPG algorithms.

Learning Outcomes:

After completion of this unit the student will be able to

- identify the various test generation methods for combinational circuits (L2).
- apply ATPG methods to discover faults at functional level (L3).
- measure controllability and observability for testability (L3).

UnitIII **8L**

Sequential Circuit Test Generation: ATPG for single-clock synchronous circuits, time-frame expansion method, simulation-based sequential circuit ATPG.

Learning Outcomes:

After completion of this unit the student will be able to

- extend combinational ATPG algorithms for test generation (L2).
- implement ATPG for cyclic and cycle-free circuits (L3).

UnitIV **8L**

Memory Test: Memory density and defect trends, faults, memory test levels, march test notation, fault modeling, memory testing Digital DFT and Scan Design: Ad Hoc DFT methods, scan design, partial- scan design, variations of scan.

Learning Outcomes:

After completion of this unit the student will be able to

- separate memory fault types at different test levels (L1).
- build fault models for memory test (L2).
- distinguish various Scan methods for test generation and application in DFT (L3).

UnitV **8L**

Built-In Self-Test: The economic case for BIST, random logic BIST, memory BIST, delay fault BIST. Boundary Scan Standard: Motivation, system configuration with boundary scan, boundary scan description language.

Learning Outcomes:

After completion of this unit the student will be able to

- Discuss BIST architecture(L1)
- Classifydifferent BIST Techniques used for Test Generation(L1)
- Explain operation of elementary boundary scan cell(L2)
- Identify boundary scan descriptive language for implementing boundary scan in any device(L3)

Text Book

1. M. L. Bushnel, V. D. Agarwal, Essentials of Testing for Digital, Memory andMixed-Signal VLSI Circuits, Kluwer Academic Publishers,2012.

References

1. M. Abramovici, M. A. Breuer, & A. D. Friedman, Digital Systems Testing and TestableDesign, IEEEPress,2011.

2. Niraj Jha, Sandeep Gupta, Test of Digital Systems, Cambridge University Press,2010.
3. Robert J. Feugate, Steven M. McIntyre, Introduction to VLSI Testing, Prentice Hall of India, 2010.

Course Outcomes:

Successful completion of the course, the student will be able to

- acquire knowledge about fault modeling and collapsing (L1).
- learn about various combinational ATPG (L2).
- understand sequential test pattern generation (L2).
- use various techniques such as BIST and Boundary scan (L3).

19EES752: CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

L	T	P	C
3	0	0	3

This course introduces the students, to digital system design with programmable devices. The first two units cover programmable deices of PAL, PLA, CPLD and FPGA. The next two units cover the differences among SRAM based FPGA and anti-fuse FPGA. The last unit covers the design of adders and counters with FPGA.

Course objectives:

1. To understand different programmable devices available for digital system design
2. To understand the architecture FPGA, programming and its applications
3. To study about different SRAM type FPGAs
4. To study about different anti fuse type FPGAs
5. To understand the programming of FPGA for various applications

UnitI **9L**

Introduction to Programmable Logic Devices: Introduction, simple programmable logic device, read only memories, programmable logic arrays, programmable array logic, programmable logic devices/generic array logic; complex programmable logic devices. Architecture of Xilinx cool runner XCR3064XL CPLD, CPLD implementation of a parallel adder with accumulation.

Learning Outcomes:

After completion of this unit the student will be able to

- compare programmable logic device PLA, PAL, CPLD (L2).
- demonstrate the need for programmable devices in the design of digital IC's (L2).
- build parallel adder with accumulation with Xilinx CPLD (L3).

UnitII **9L**

Field Programmable Gate Arrays: Organization of FPGAs, FPGA programming technologies, programmable logic block architectures, programmable interconnects, programmable I/O blocks in FPGAs, dedicated specialized components of FPGAs, applications of FPGAs.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the architecture of FPGA (L2).
- show the FPGA programming (L2).
- spell the applications of FPGA (L1).

UnitIII **8L**

SRAM Programmable FPGAs: Introduction, advantages and disadvantages of SRAM programming, design tradeoffs, programming technology, device architecture, the XilinxXC2000, XC3000 and XC4000 architectures, programming the FPGA, automated design implementation, technology specific synthesis.

Learning Outcomes

After completion of this unit the student will be able to

- explain the advantages and disadvantages of SRAM programming (L2).
- compare XC2000, XC3000 andXC4000 architectures (L2).
- outline programming the SRMA FPGA and synthesis (L1).

UnitIV **8L**

Anti-Fuse Programmed FPGAs: Introduction, programming technology, device architecture, routing architecture of the Actel FPGA, The Actel ACT1, ACT2 and ACT3 Architectures, programming and testing, performance, capacity, synthesis design flow.

Learning Outcomes:

After completion of this unit the student will be able to

- what is the purpose of Anti-Fuse Programmed FPGA (L1).
- compare Actel ACT1, ACT2 and ACT3 Architectures (L2).
- summarize the design flow (L2).

UnitV **8L**

Design Applications: General design issues, counter examples, a fast video controller, a position tracker for a robot manipulator, a fast DMA controller, designing counters with ACT devices, designing adders and accumulators with the ACT architecture.

Learning Outcomes:

After completion of this unit the student will be able to

- build DMA controller in FPGA (L1).
- experiment with ACT devices and can design counters (L3).
- utilize ACT devices to develop adders and accumulators (L3).

Text Books:

1. Stephen M. Trimberger, Field Programmable Gate Array Technology, Springer International Edition, 1994.
2. Charles H. Roth Jr, Lizy Kurian John, Digital Systems Design, CengageLearning,1998.

References

1. John V. Oldfield, Richard C. Dorf, Field Programmable Gate Arrays, WileyIndia.
2. PakK.Chan,SamihaMourad,DigitalDesignUsingFieldProgrammableGateArrays,Pearson, 2011.
3. Ian Grout, Digital Systems Design with FPGAs and CPLDs, Elsevier,Newnes, 2008.
4. Wayne Wolf, FPGA based System Design, Prentice Hall Modern Semiconductor Design Series,2004

Course Outcomes:

successful completion of the course, the student will be able to

- understand about the differences PAL, PLA, CPLD (L1).
- understand the FPGA architecture programming and applications (L2).
- understand the variations in SRAM based FPGAs (L3).
- understand the variations in Anti fuse based FPGAs (L4).
- understand the design of combinational and sequential circuit design with FPGA (L5).

19EES754: DSP PROCESSORS

L	T	P	C
3	0	0	3

This course introduces the students, to architecture and interfacing of DSP processors to develop DSP applications. The first unit covers the review of DSP processing techniques and computational errors due to A/D and D/A converters. The next two units cover the super Harvard architecture of DSP processors and programming of TMS processors. The last two units cover pipelining concept in DSP processors and interfacing peripherals.

Course objectives:

1. To review the basic concepts of DSP and realize the significance of computational accuracy in DSP implementations.
2. To learn various architectures for programmable DSP devices.
3. To understand the architecture, instruction set and programming of programmable digital signal processors.
4. To analyze the concepts of execution control and pipelining.
5. To acquire knowledge to interface memory and peripherals to programmable digital signal processors

UnitI **9L**

Review of Digital signal processing: Introduction to digital signal processing, the sampling process, Discrete time sequences, discrete Fourier transform and FFT, Linear time –invariant systems, digital filters, decimation and Interpolation. **Computational accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate the sampling theorem and DSP processing such as FFT and DSP filters (L2).
- explain the IEEE number formats of digital signals (L2).
- identify the errors due to ADC and DAC converters(L3).

UnitII **8L**

Architectures for programmable DSP devices: Basic architectural features, DSP computational building blocks, Bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Learning Outcomes:

After completion of this unit the student will be able to

- Illustrate the architecture of DSP processors, features and building blocks (L2)
- Choose addressing modes in DSP devices(L3)
- Relate speed issues and program execution(L2)

UnitIII **8L**

Programmable Digital Signal Processors: Introduction, commercial digital signal processing devices, the architecture of TMS320C54xx digital signal processors, addressing modes of the TMS320C54xx processors, memory spaces of TMS320C54xx processors, program control, TMS320C54xx instructions and programming, on-chip peripherals. Interrupts, pipeline operation of the TMS320C54xx processors.

Learning Outcomes:

After completion of this unit the student will be able to

- examine the architecture of TMS320C54xx digital signal processors and addressing modes (L4).
- experiment with o on-chip peripherals programming (L3).
- plan for interrupts and pipeline operations (L3).

UnitIV **8L**

Execution control and Pipelining: hard ware looping, Interrupts stacks, relative branch support, pipelining and performance, Pipeline depth, interlocking, branching effects, Interrupt effects, Pipeline programming models.

Learning Outcomes:

After completion of this unit the student will be able to

- build hardware looping with TMS processors (L3).
- develop interrupts programming (L3).
- model Pipeline programming (L3).

UnitV **9L**

Interfacing Memory and Peripherals to Programmable DSP devices: Memory space organization, External bus interfacing signals, Memory interface, parallel I/O interface, programmable I/O, Interrupt and I/O, direct memory access. Multichannel buffered serial port (McBSP).

Learning Outcomes:

After completion of this unit the student will be able to

- make use of memory space in DSP processors (L3).
- demonstrate DMA (L2).
- develop Peripherals to Programmable DSP devices (L3).

Text Book

1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Cengage Learning, India, 2012.

References

1. Rulph Chassaing, Digital Signal Processing with C6713 and C6416 DSK, 2/e Wiley Publications, 2013.
2. DSP processor fundamentals, Architecture & Features-Lapsley et al. S. Chand & Co,2012.
3. Steve Tretter, Communication System Design using DSP Algorithms, Springer Publications,2011.

Course Outcomes

successful completion of the course, the student will be able to

- summarize the basic concepts and realize the impact of computational accuracy in DSP implementations (L1)
- understand the computational blocks for different programmable DSP devices (L2).
- identify the architectural highlights of programmable digital signal processors (L3).
- explore the effects of execution control and pipelining (L4).
- understand the interfacing of memory and peripherals to programmable digital signal processors (L5).

19EES756: EMBEDDED LINUX

L	T	P	C
3	0	0	3

This course introduces the students; to embedded systems develop applications using linux programming. The first unit covers the basic concepts of linux and its architecture. The next two units cover linux tools chain and linux kernel insights. The last two units cover file management in linux and memory management.

Course objectives:

1. To study about the generic architecture of an embedded linux system and basic concepts of LINUX.
2. To study about the buses, I/O interfaces, Programming languages implementation in LINUX.
3. To study about the LINUX Kernel and basic terminology in embedded linux.
4. To study about the file systems, library, boot loader and universal boot loader in embedded linux.
5. To study about the storage device manipulation in embedded linux.

UnitI **8L**

Introduction: Definitions, real life and embedded linux systems, example multi component system, design and implementation methodology. Basic Concepts: types of hosts, types of host/target development setups, types of host/target debug setups, generic architecture of an embedded linux system, system startup, types of boot configurations, system memorylayout.

Learning Outcomes:

After completion of this unit the student will be able to

- explain the linux systems design and implementation (L2).
- summarize the linux architecture (L2).
- compare types of boot configurations in linux (L2).

UnitII **8L**

Hardware Support: Processor architectures, buses and interfaces, I/O, storage, general purpose networking, industrial grade networking, system monitoring. Development Tools: using a practical project workspace, GNU cross-platform development tool chain, C library alternatives, Java, Perl, Ada, other programming languages, integrated development environments, terminal emulators.

Learning Outcomes:

After completion of this unit the student will be able to

- classify buses and interfaces (L2).
- illustrate GNU cross-platform development tool chain and linux IDE (L2).
- tell about the use of terminal emulator (L1).

UnitIII **8L**

The Linux Kernel: Top-level source directory, compiling the kernel, the kernel proper: vm linux, kernel image components, subdirectory layout, the dot-config, make file targets, custom configuration options, kernel make files, obtaining accustomlinux kernel. Kernel Initialization, Composite kernel image: piggy and friends, the image object, architecture objects, bootstrap loader, boot messages, initialization flow of control, kernel entry point: head O, kernel startup: main.C, architecture setup, kernel command- line processing, the setup macro, subsystem initialization, the initcall macros, the init thread, initialization via initcalls, initcall debug, finalbootsteps

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate linux kernel and its functions (L2).
- explain about the layout of linux directories (L2).
- identify initialization of initcall debug, final boot steps (L3).

Unit I V **9L**

Root File System Content: Basic root file system structure, libraries, kernel Units, kernel images, device files, main system applications, custom applications, system initialization. boot loaders, role of a boot loader, boot loader challenges, DRAM controller, flash versus RAM, image complexity, execution context, a universal boot loader: Das U-Boot, obtaining U-Boot, configuring U- Boot, U-Boot monitor commands, porting U-Boot, EP405 U-Boot port.

Learning Outcomes:

After completion of this unit the student will be able to

- explain about the root file systems in linux (L2).
- demonstrate boot loading process in linux (L2).
- illustrate U-Boot and its configuring (L2).

UnitV **9L**

Storage device manipulation: MTD-supported devices, disk devices, to swap or not to swap, setting up the boot loader: boot loaders galore, server setup for network boot, using LILO with disk and compact flash devices, using grub with disk on chip devices, U-Boot.

Learning Outcomes:

After completion of this unit the student will be able to

- explain about the MTD-supported devices (L2).
- demonstrate setup for network boot (L2).
- illustrate usingLILO with disk and compact flash devices (L2).

Text Books:

1. Building Embedded Linux Systems by Karim Yaghmour, Jon Masters, Gilad Ben- Yossef, Philippe Gerum, 2/e, O'ReillyMedia,2008.
2. Embedded Linux Primer:35A Practical Real-World Approach, Christopher Hallinan, 2/e, Prentice Hall,2011.

Course Outcomes:

successful completion of the course, the student will be able to

- the student will be able to understand the architecture of an embedded linux system (L1).
- the student will be able to understand the Programming languages implementation in Embedded linux (L2).
- the student will understand the linux kernel and terminology in embedded linux (L3).
- the student will be able to understand the creation of files and loading the universal boot loader in the processor (L4).
- the student will be able to understand the storage device manipulation in embedded linux (L5).

19EES758: FUNDAMENTALS AND APPLICATIONS OFMEMS

L	T	P	C
3	0	0	3

This course introduces the students, to structure of MEMS and MEMS technologies and applications of MEMS. The first two units cover basic structure of MEMS and mechanical design aspects. The next two units cover two terminals and three terminal MEMS and RF MEMS design. The last MEMS technologies and process flow such as bulk and surface micromachining.

Course objectives:

1. To study the basic structures of MEMS devices and their response to different stimuli.
2. To know the properties of MEMS structures for various excitations.
3. To study two terminals and three terminal MEMS structures and their applications.
4. To develop basic gates using different MEMS structures and to study MEMS based transducers.
5. To acquire knowledge on silicon and metal based MEMS fabrication

Unit I **8L**

Introduction, basic structures of MEM devices: (Canti levers, fixed beams diaphragms), broad response of micro electromechanical systems (MEMs) to mechanical (force, pressure etc.) thermal, electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

Learning Outcomes:

After completion of this unit the student will be able to

- demonstrate the structure of MEMS, and canti levers, fixed beams diaphragms (L2).
- illustrate the stimuli in MEMs (L2).
- spell power dissipation, leakage problems (L1).

Unit II **9L**

Review of mechanical concepts: Stress, strain, bending moment, deflection curve, differential equations describing the deflection under concentrated force, distributed force, deflection curves for canti levers, fixed beam. electrostatic excitation, columbic force between the fixed and moving electrodes, deflection with voltage in C.L, deflection vs voltage curve, critical fringe fields, field calculations using Laplace equation, discussion on the approximate solutions, transient response of the MEMS.

Learning Outcomes:

After completion of this unit the student will be able to

- outline stress, strain and force deflection curves of cantilever beam (L2).
- show the calculations using Laplace equation of cantilever beam (L2).
- explain transient response of the MEMS (L2).

Unit III **8L**

Two terminal MEMS: Capacitance vs voltage curve, variable capacitor, applications of variable capacitors, two terminal MEM structures, three terminal MEM structures, controlled variable capacitors, MEM as a switch and possible applications.

Learning Outcomes:

After completion of this unit the student will be able to

- compare two terminals and three terminal MEMS (L2).
- infer the MEM as a switch and possible applications (L2).
- explain Capacitance vs voltage curves of two and three terminal MEMS (L2).

Unit IV **9L**

MEM circuits & structures for simple gates: AND, OR, NAND, NOR, exclusive OR, simple MEM configurations for flip-flops triggering, applications to counters, converters, applications for analog circuits like frequency converters, wave shaping. RF switches for modulation, MEM transducers for pressure, force temperature, optical MEMS.

Learning Outcomes:

After completion of this unit the student will be able to

- build simple gates such as AND, OR, NAND, NOR etc (L3).
- construct flip-flops and counters (L3).
- model RF switches (L3).

Unit V **8L**

MEM technologies: Silicon based MEMS, process flow, brief account of various processes and layers like fixed layer, moving layers, spacers etc., etching technologies. Metal based MEMS: thin and thick film technologies for MEMS, process flow and description of the processes, status of MEMS in the current electronics scenario.

Learning Outcomes:

After completion of this unit the student will be able to

- outline the MEM technologies and various etching processes (L2).
- explain Process flow (L2).
- tell Status of MEMS in the current electronics scenario (L1).

Text Books:

1. Gabriel.M.Review, R.F. MEMS Theory, Design and Technology, John Wiley andSons,2003.
2. Thimo Shenko, Strength of Materials, CBS Publishers & Distributors,2000.

References

1 RisticL.(Ed.),SensorTechnologyand Devices,Artech House,London1994.
2 Servey E.Lyshevski, MEMS and NEMS, Systems Devices; and Structures, CRC Press,2002.

Course Outcomes:

successful completion of the course, the student will be able to

- understand the response characteristics of MEMS based Cantilevers and fixed beam diaphragms for different types of inputs (L1).
- understand the performance characteristics and transient response of MEMS structures(L2).
- understand the characteristics of two and three terminal MEMS based capacitive structures (L3).
- realize MEMS based basic gates and familiar with MEMS transducers for temperature and pressure measurement (L4).
- understand current trends in thin and thick film MEMS fabrication processes (L5).

19EOE742: BUSINESS ANALYTICS

L	T	P	C
3	0	0	3

This course introduces students to the science of business analytics. The goal is to provide students with the foundation needed to apply data analytics to real-world challenges they confront daily in their professional lives. Students will learn to identify the ideal analytic tool for their specific needs; understand valid and reliable ways to collect, analyze, and visualize data; and utilize data in decision making for managing agencies, organizations or clients in their workspace

Course Objectives:

- To familiarize the scope, process and advantages of business analytics
- To acquaint the student with the modeling and problem solving skills in business analytics
- To impart the organization and management of business analytics
- To introduce the forecasting models and techniques used in analytics
- To expose the formulation and decision strategies used in business analytics

Unit I **8L**

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the scope and process of business analytics (L1).
- choose an organizational structure to implement a business analytics process (L4).
- describe the statistical tools and methods used for data modeling and analysis (L2).
- identify the sampling and estimation requirements for data analysis (L1).

Unit II **8L**

Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

Learning Outcomes:

After the completion of this unit, the student will be able to

- identify the relationships and trends in data (L1).
- utilize linear regression methods for identifying data relationships (L4).
- list the types of data and their models used for business analytics (L1).
- describe the methods for visualization and exploration of data (L2).

Unit III **8L**

Organization Structures of Business analytics: Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the management issues in the organization structures (L2).
- define the designing information policy and its usage (L1).
- list the methods for ensuring data quality measuring contribution (L1).
- explain the use of data mining methodologies for predictive analytics analysis (L3).
- describe the use of prescriptive analytics methods in business analytics process (L2).

Unit IV **10L**

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Learning Outcomes:

After the completion of this unit, the student will be able to

- classify and describe the use of forecasting models (L3).
- model the use of regression forecasting with casual variables (L5).
- identify the appropriate forecasting model for a given data (L5).
- explain the use of monte carlo simulation for forecasting and identify the involved risk (L2).

Unit V **8L**

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

Learning Outcomes:

After the completion of this unit, the student will be able to

- formulate decision problems (L2).
- list the decision strategies with and without probabilities (L1).
- use the decision trees for analysis (L4).
- describe the value of information, utility and its use in decision making (L4).

Textbook(s):

1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Business analytics Principles, Concepts, and Applications Pearson FT Press, 2014.
2. James Evans, Business Analytics, Pearson Education, 2013.

Course Outcomes:

Upon successful completion of the course, the student will be able to

- define the scope, process and advantages of business analytics (L1).
- explain the modeling and problem solving skills in business analytics (L2).
- describe the organization and management of business analytics (L3).
- utilize the forecasting models and techniques used in analytics (L4).
- enumerate and utilize the formulation and decision strategies (L2).

19EOE746: OPERATIONS RESEARCH

L	T	P	C
3	0	0	3

Optimization problems arise in all walks of human activity- particularly in engineering, business, finance and economics. The simplest optimization problems are linear in nature which may be subject to a set of linear constraints. This course will equip the student with the expertise to mathematically model real life optimization problems as Linear Programming (Optimization) Problems and subsequently educate the student to solve these models with the help of the available methods.

Course Objectives:

- To impart knowledge on developing mathematical formulation for linear programming and transportation problem
- To familiarize the student in the construction of the required activities in an efficient manner to complete it on or before a specified time limit and at the minimum cost.
- To expose the development of mathematical model for interactive decision-making situations, where two or more competitors are involved under conditions of conflict and competition.
- To illustrate PERT and CPM techniques for planning and implementing projects.
- To impart the knowledge of formulating and analysis of real life problems using advanced tools and techniques for resource optimization.
- To provide frameworks for analyzing waiting lines using advanced queuing theory concepts.

Unit I **8L**

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Learning Outcomes:

After completing this unit, the student will be able to

- identify and develop operational research models from the verbal description of the real system (L4).
- understand the classification systems of effective Inventory control models (L2).

Unit II **8L**

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Learning Outcomes:

After completing this unit, the student will be able to

- translate a real-world problem, given in words, into a mathematical formulation (L2)
- utilize the mathematical tools that are needed to solve optimization problems (L2)

Unit III **8L**

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Learning Outcomes:

After completing this unit, the student will be able to

- describe the need and origin of the optimization methods (L2).
- classify optimization problems to suitably choose the method needed to solve the particular type of problem (L3).

Unit IV **8L**

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Learning Outcomes:

After completing this unit, the student will be able to

- choose linear programming problems to suitably choose the method needed to solve the particular type of problem (L1).
- identify industrial problems involved in inventory, MRP and scheduling (L2).

Unit V **8L**

Competitive Models, Single and Multi-Channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

Learning Outcomes:

After completing this unit, the student will be able to

- identify the values, objectives, attributes, decisions, uncertainties, consequences, and trade-offs in a real decision problem (L2).
- apply the models to incorporate rational decision-making process in real life situations (L3).
- analyze various modeling alternatives & select appropriate modeling techniques for a given situation (L3).

Text Book(s):

1. H.A. Taha, Operations Research, An Introduction, Prentice Hall of India, 2008
2. H.M. Wagner, Principles of Operations Research, Prentice Hall of India, Delhi, 1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, 2008
4. Hitler Libermann Operations Research: McGraw Hill Publishers, 2009
5. Pannerselvam, Operations Research: Prentice Hall of India, 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India, 2010

Course Outcomes:

After the successful completion of the course, the students will be able to

- Understand the basic concepts of different advanced models of operations research and their applications (L2).
- Solve linear programming problems using appropriate techniques and optimization solvers, interpret the results obtained and translate solutions into directives for action (L4).
- Apply the models to incorporate rational decision-making process in real life situations (L4).
- Analyze various modeling alternatives & select appropriate modeling techniques for a given situation (L3).
- Validate output from model to check feasibility of implementations (L5).
- Create innovative modeling frameworks for a given situation (L6).
- Conduct and interpret post-optimal and sensitivity analysis and explain the primal-dual relationship (L3).

19EOE748: COST MANAGEMENT OF ENGINEERING PROJECTS

L	T	P	C
3	0	0	3

This course will equip the student with the expertise to mathematically model engineering projects and use effective methods and techniques to plan and execute engineering activities.

Course Objectives:

- To introduce the basic principles of strategic cost management and the related terminology
- To familiarize the project planning and execution process involving technical/nontechnical activities
- To acquaint the student with detailed engineering activities and their cost management analysis
- To impart the knowledge of cost analysis and profit planning of engineering projects
- To familiarize the quantitative techniques for optimization of budget allocation

Unit I **8L**

Introduction and Overview of the Strategic Cost Management Process, Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational
control; Provision of data for Decision-Making.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the cost concepts in decision making (L2).
- define the various costs involved in the cost management process (L2).
- list the objectives of cost control (L2).
- identify the different fields of a database for operational control (L2).

Unit II **8L**

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities.

Learning Outcomes:

After the completion of this unit, the student will be able to

- define the meaning of a project and list the different types (L2).
- identify the measures to manage cost overruns (L2).
- describe the various stages of project execution from conception to commissioning (L2).
- plan the proper order of technical/nontechnical activities as part of project execution (L2).

Unit III **8L**

Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

Learning Outcomes:

After the completion of this unit, the student will be able to

- identify the different clearance norms required in the pre-project execution phase (L2).
- describe the hierarchy of project team and identify the role of each member (L2).
- list the different contents of project contracts (L2).
- present the project cost control and planning through bar charts, network diagrams etc (L2).

Unit IV **8L**

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis.

Learning Outcomes:

After the completion of this unit, the student will be able to

- describe the cost behavior and profit planning (L2).
- distinguish between marginal costing and absorption costing (L2).
- analyze the variance of standard costing (L2).
- analyze the pricing strategies in project costing (L2).
- identify the quality measures satisfying the appropriate constraints (L2).

Unit V **10L**

Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing. Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory

Learning Outcomes:

After the completion of this unit, the student will be able to

- define and compare the different budgeting strategies (L2).
- model the cost management as a linear programming problem (L2).
- measure the divisional profitability and decide the appropriate pricing (L2).

Textbook(s):

1. Charles T. Horngren, Srikant M. Datar, George Foster, Cost Accounting a Managerial Emphasis, Prentice Hall of India, New Delhi, 2006.

References:

1. Charles T. Horngren, George Foster, Advanced Management Accounting, Greenwood Publishing, 2001.
2. Robert S Kaplan, Anthony A. Alkinson, Management & Cost Accounting, 1998.
3. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting, Wheeler Publisher, 2004.
4. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book, 2006.

Course Outcomes:

After the successful completion of the course, the students will be able to

- list the basic principles of strategic cost management and define the related terminology (L1).
- plan the project execution process involving technical/nontechnical activities (L4).
- describe the detailed engineering activities and their cost management analysis (L2).
- carry out the cost analysis and profit planning of engineering projects (L5).
- utilize quantitative techniques for optimization of budget allocation (L6).

19EOE752: WASTE TO ENERGY

L	T	P	C
3	0	0	3

This course introduces the basic principles and different technologies of converting waste to energy. Student will be able to appropriately identify the methods and build biomass gasification systems of different capacities depending on application requirements.

Course Objectives:

- to introduce the classification of waste for its usefulness in preparing different fuels
- to familiarize the biomass pyrolysis process and its yield issues
- to acquaint the student with biomass gasification processes and construction arrangements
- to impart the types and principles of biomass combustors
- to familiarize the calorific values and composition of biogas resources

Unit I **8L**

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

Learning Outcomes:

After the completion of this unit, the student will be able to

- distinguish between different types of waste (L1).
- classify the different types of waste for manufacturing different types of fuel (L3).
- identify the different conversion devices and their applications (L4).

Unit II **8L**

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

Learning Outcomes:

After the completion of this unit, the student will be able to

- classify the different types of pyrolysis methods based on speed (L1).
- describe the different methods of manufacturing charcoal (L2).
- explain the chemical processes involved in the manufacture of pyrolytic oils and gases (L2).

Unit III **8L**

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic
consideration in gasifier operation.

Learning Outcomes

After the completion of this unit, the student will be able to

- explain the design, construction and operation of different gasifiers (L2).
- describe the burner arrangement for thermal heating (L2).
- elaborate the gasifier engine arrangement for equilibrium and kinetic considerations (L3).

Unit IV **8L**

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

Learning Outcomes:

After the completion of this unit, the student will be able to

- explain the basic principle of biomass combustors (L2).
- classify different combustors based on their capacity and efficiency (L3).
- describe the construction and operation of fixed bed inclined grate, fluidized bed combustors (L2).

Unit V **10L**

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Learning Outcomes:

After the completion of this unit, the student will be able to

- list the properties of biogas (L1).
- elaborate the design, construction and operation of biogas plant (L2).
- classify the different biomass resources and their conversion process (L3).
- distinguish between different biogas plants and identify their applications (L5).

Text Book(s)

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

Course Outcomes:

After the successful completion of the course, the student will be able to

- classify different types of waste for their usefulness in preparing different fuels (L3).
- describe the biomass pyrolysis process and its yield issues (L2).
- outline the different biomass gasification processes and their construction arrangements (L3).
- explain the types and principles of biomass combustors (L2).
- analyze the calorific values and composition of biogas resources (L5).

19EES792: TECHNICAL SEMINAR

L	T	P	C
0	0	4	2

Each student shall survey a technical topic related to a chosen specialization and prepare/submit a report in a specified format. Each student has to prepare a power point presentation on a selected technical topic with a novelty and get it evaluated by the faculty assigned for this purpose.

19EES722: EMBEDDED SYSTEM LABORATORY

L T P C
0 0 4 2

Course Objectives

1. To develop programs in C and assembly language for advanced 32-bit microcontroller
2. To learn about the use of LPC 2148 ARM microcontroller peripherals to develop embedded systems.
3. To learn design of external interfacing of devices to ARM microcontroller.
4. To learn how to use Vxworks RTO's.
5. To develop programs Vxworks for IPC synchronization.

1. Blinking led with 1 sec delay using ARM7 microcontroller by software delay method (both slow GPIOand Fast GPIO)
2. Timer programming of ARM7 microcontroller to generate 1 sec delay using polling method
3. Timer programming of ARM7 microcontroller to generate 1 sec delay using Interrupt method
4. UART programming of ARM7 microcontroller to transmit string to HyperTerminal.
5. ADC programming of ARM7microcontroller.
6. SPI programming of ARM7microcontroller.
7. I2C programming of ARM7microcontroller.
8. DC motor control using ARM7microcontroller
9. Internet based control of LEDsusingARM9 microcontroller.
10. Vxworks - Signals & tasks programming
11. Vxworks – Semaphore programming
12. Vxworks - Interrupts programming
13. Vxworks - Message queue programming
14. Vxworks - Priority inversion programming

Course Outcomes

successful completion of the course, the student will be able to

- Develop advanced 32 bit ARM microcontroller LPC 2148 programs for control of leds using Keil software and can debug
- Design programs with polling and interrupt method for LPC218 microcontroller.
- Write point to point data communication with LPC2148.
- Write programs semaphore and signal programs using Vxworks.
- Develop programs to message queues with Vxworks.

19EES724: DIGITAL VLSI DESIGN LABORATORY

L	T	P	C
0	0	4	2

Course Objectives

1. To understand Analog IC design with SPICE CAD tools
2. Tocarry simulation and transient analysis of electronic components.
3. Toanalyze the I-V Curves of transistors.
4. To learn dynamic characteristics of CMOS circuits.
5. To test and verify the programs developed Xilinx and Modelsim software.

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer FunctionAnalysis)
2. Modeling of Diodes usingSPICE.
3. Modeling of MOS transistors, Bipolar Transistors usingSPICE.
4. I-V Curves of NMOSTransistors.
5. I-V Curves of PMOSTransistors
6. DC Characteristics of CMOS Inverters (VTC, NoiseMargin).
7. Dynamic Characteristics of CMOS Inverters (Propagation Delay, PowerDissipation).
8. Schematic Entry/Simulation/ Layout of CMOS CombinationalCircuits.
9. Schematic Entry/Simulation/ Layout of CMOS SequentialCircuits.
10. High Speed and Low Power Design of CMOSCircuits.
11. Modeling and Functional Simulation of the digital circuits (with Xilinx/ModelSim tools) using VHDL/Verilog Hardware Description Languages) likeMultiplexer, Comparator, Adder/Subtractor.
12. Modeling and Functional Simulation of the digital circuits (with Xilinx/ModelSim tools) using VHDL/Verilog Hardware Description Languages) like D-Flip Flop, JK-FlipFlop.

Course Outcomes

successful completion of the course, the student will be able to

- Develop programs for modeling diodes and transistors and also can perform transient analysis
- Design flip flops and counters in Verilog using Xilinx software.
- Write the programs with Schematic Entry/Simulation/ Layout of CMOS CombinationalCircuits.
- Write and test the programs for NMOS and PMOS transistors.
- Develop application to design analog ICS with SPICE.

19EES891: PROJECT WORK I

L	T	P	C
0	0	26	13

Each student is required to submit a report of first part of project work i.e. about the problem definition, literature review and methodology to be adopted including experiments and tests to be performed on topic of project as per the guidelines decided by the department. The project work is to be evaluated through Presentations and Viva-Voce during the semester end.

19EES892: PROJECT WORK II

L	T	P	C
0	0	26	13

Each student is required to submit a detailed project report about the work on topic of project as per the guidelines decided by the department. The project work is to be evaluated through Presentations and Viva-Voce during the semester and Final evaluation will be done at the end of semester as per the guidelines decided by the department from time to time. The candidate shall present/publish one paper in national/international conference/seminar/journal of repute. However, candidate may visit research labs/institutions with the due permission of chairperson on recommendation of supervisor concerned.